

Compal Confidential

VAL40 MB Schematic Document

LA-8226P

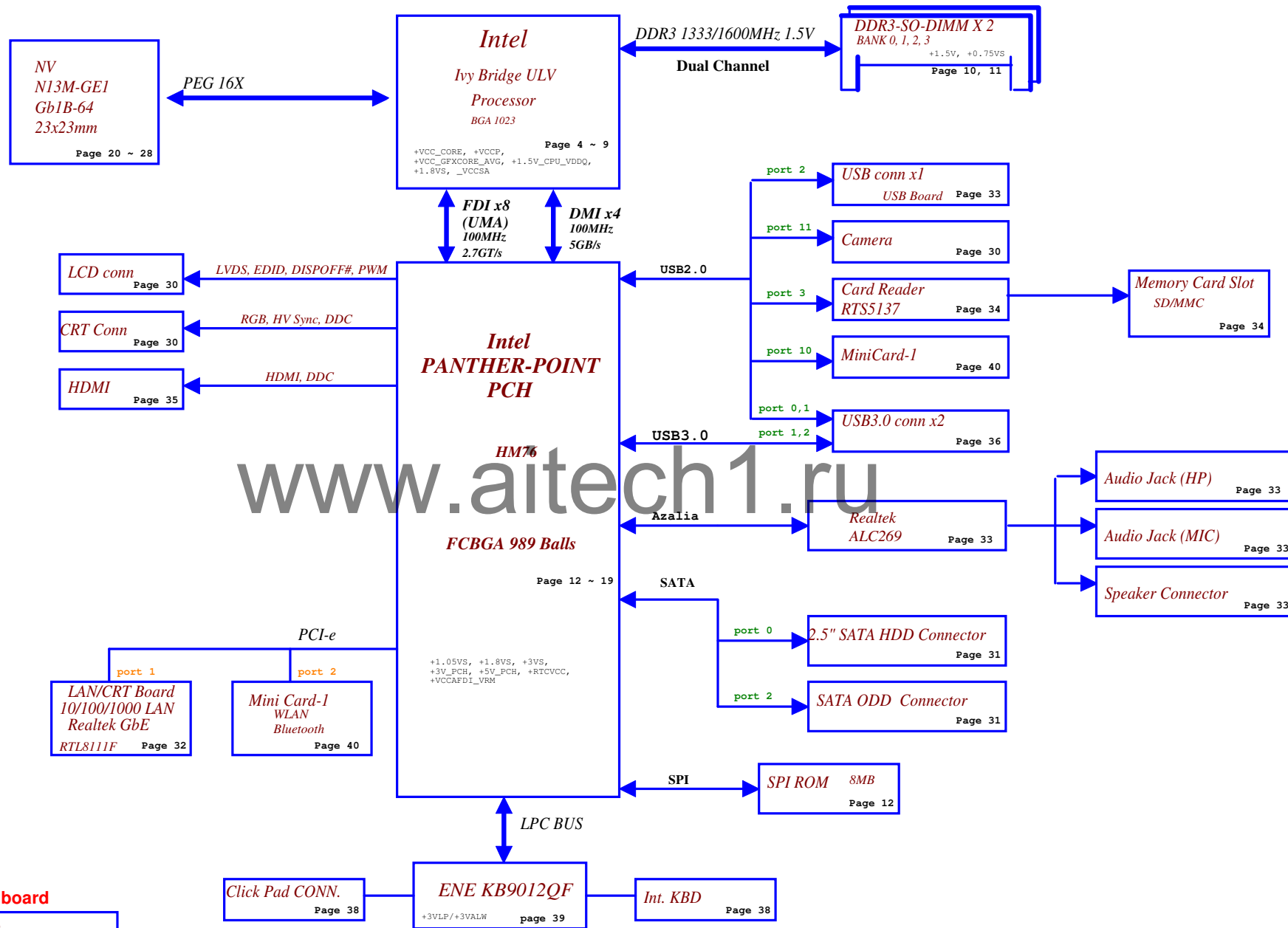
Rev: 1.0

2012.07.06

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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	Cover Sheet
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BTO Option Table

BOM Structure	BTO Item
DIS@	VGA componet
GE8@	N13M-GE1_GB1b-64
X76L07@	VRAM Hynix 2Gbx8 256Mx8
GCLK@	G-CLK
GCLKDIS@	G-CLK + SLG3NB300
GCLKUMA@	G-CLK + SLG3NB244
NONGCLK@	NONE G-CLK
AI@	AI Charger
NAI@	Non AI Charger
46@	HDMI royalty rule
I33110@	CPU BGA I3-3110M 2.4G/3M
I32370@	CPU BGA I3-2370M 2.4G/3M
I32350@	CPU BGA I3-2350M 2.3G/3M

CPU BOM Config

I33310@	I3-3110M	CR	2.4G	SA00005M830 (INT I3-3110M 2.4G/3M SR0N2 BGA)
I32370@	I3-2370M	HR	2.4G	SA000059160 (INT I3-2370M 2.4G/3M SR0DQ BGA)
I32350@	I3-2350M	HR	2.3G	SA00004QXA0 (INT I3-2350M 2.3G/3M SR0DQ BGA)

BOM Config : DIS

K45B (i3-3110M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I33110@/NAI@

* K45B (i3-2370M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I32370@/NAI@

BOM Config : UMA

K45B (i3-3110M) GCLK@/GCLKUMA@/I33110@/NAI@

K45B (i3-2370M) GCLK@/GCLKUMA@/I32370@/NAI@

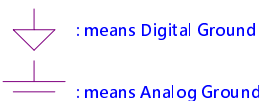
* K45B (i3-2350M) GCLK@/GCLKUMA@/I32350@/NAI@

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

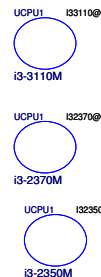
Symbol Note :



VRAMX8X8



CPU



CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

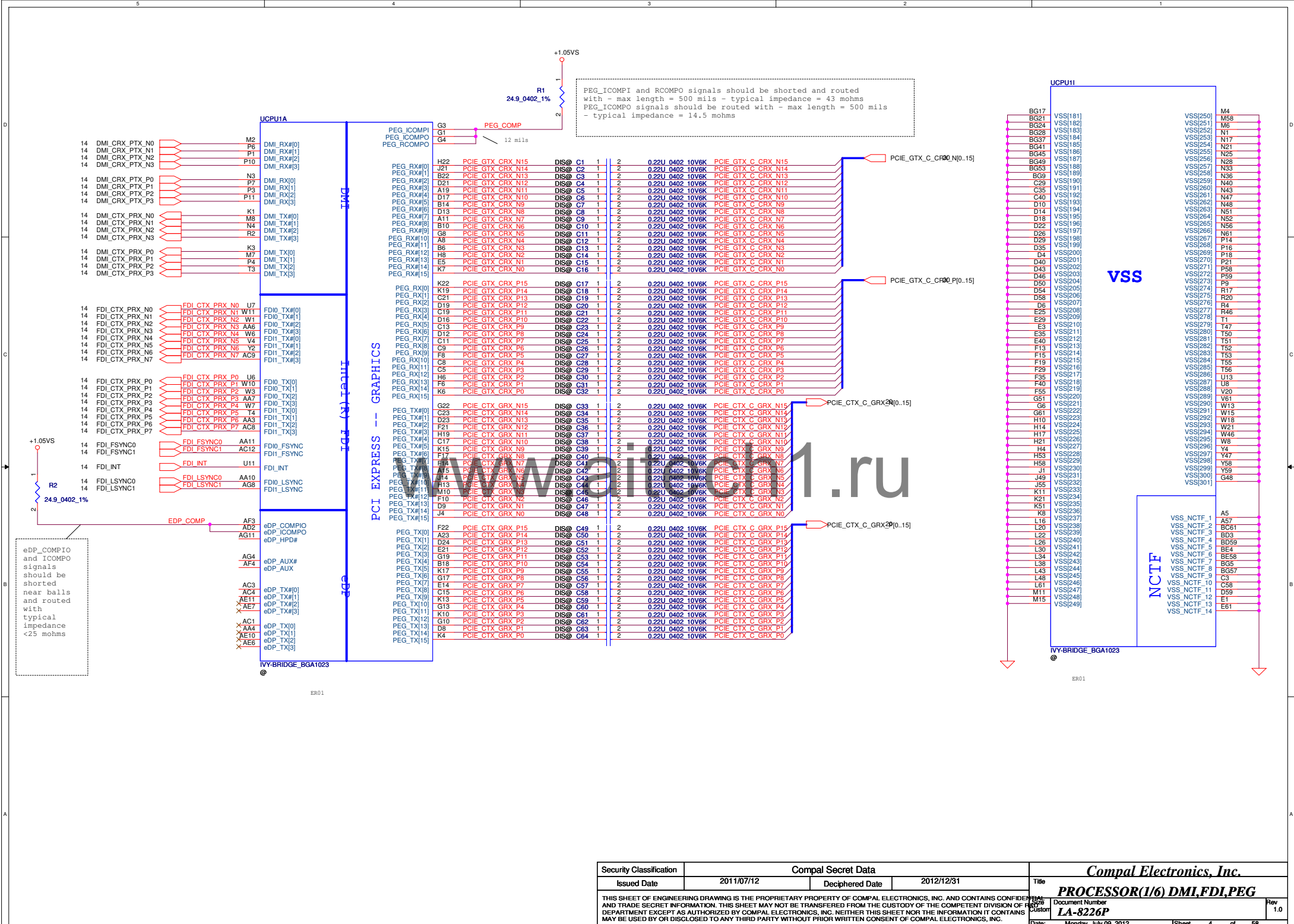
Voltage Rails

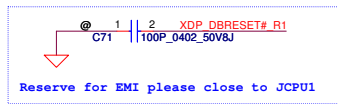
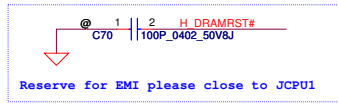
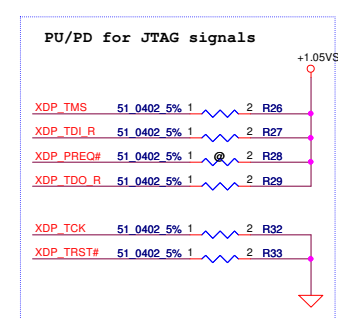
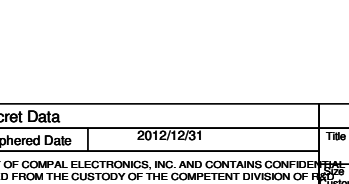
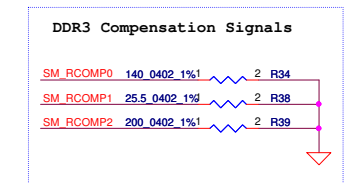
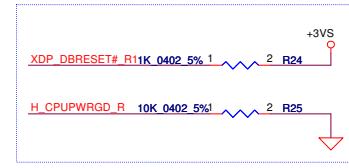
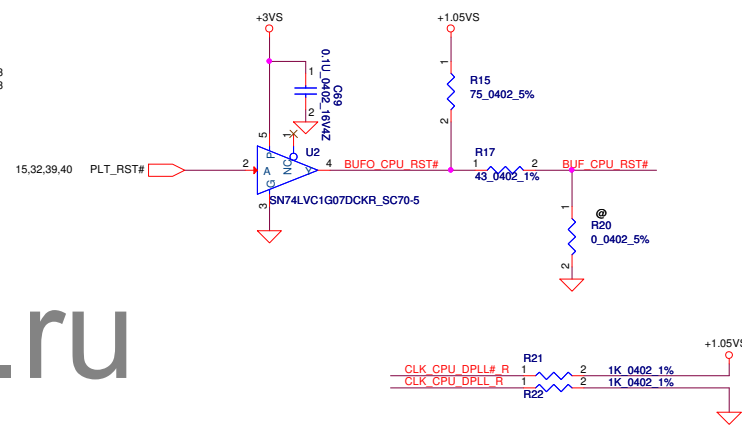
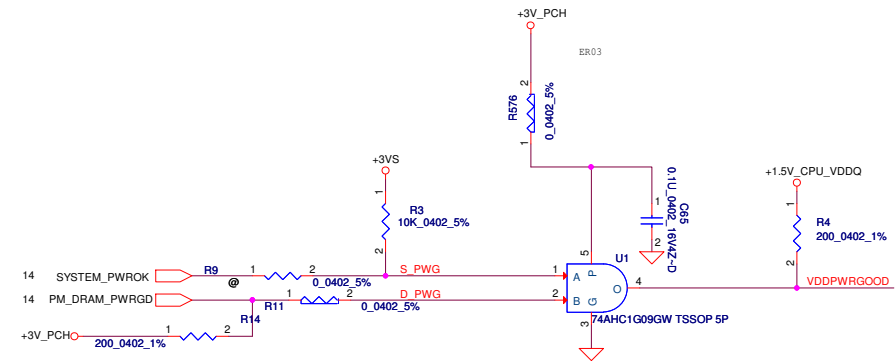
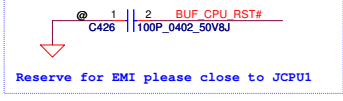
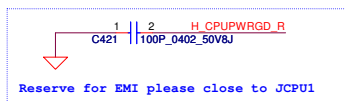
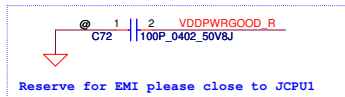
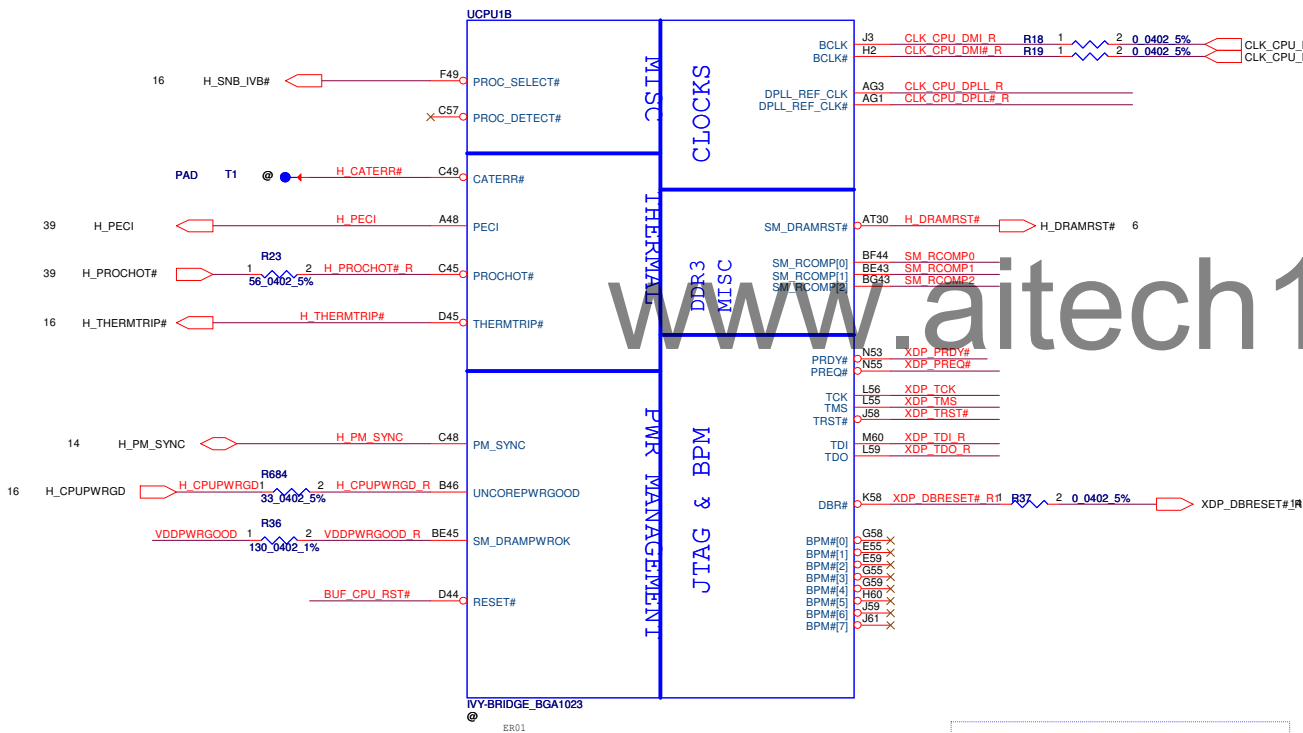
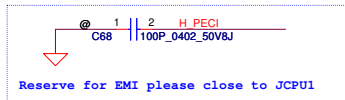
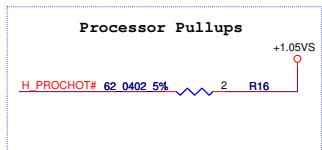
Power Plane	Description	S0	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORR_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

USB2 PORT	DESTINATION
0	USB2.0+3.0
1	USB2.0+3.0
2	USB2
3	Card Reader
4	None
5	None
6	None
7	None
8	None
9	None
10	JMINI1 (WLAN) Bluetooth
11	CAMERA
12	None
13	None

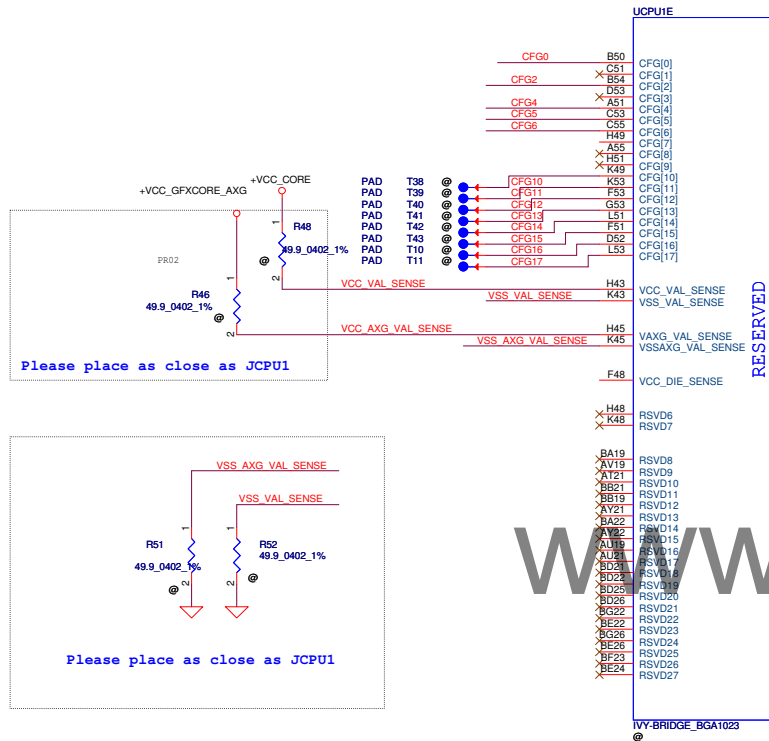
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



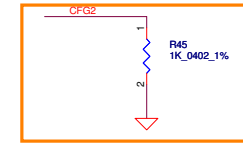


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Deciphered Date				2012/12/31				PROCESSOR(2/6) PM,XDP,CLK			
Document Number				LA-8226P				Rev			
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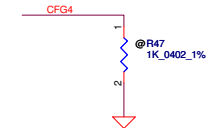
CFG Straps for Processor



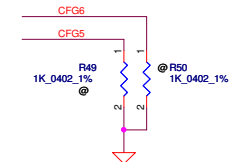
These pins are for solder joint reliability and non-critical to function. For BG only.



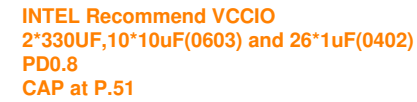
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



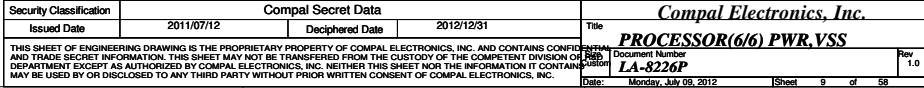
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

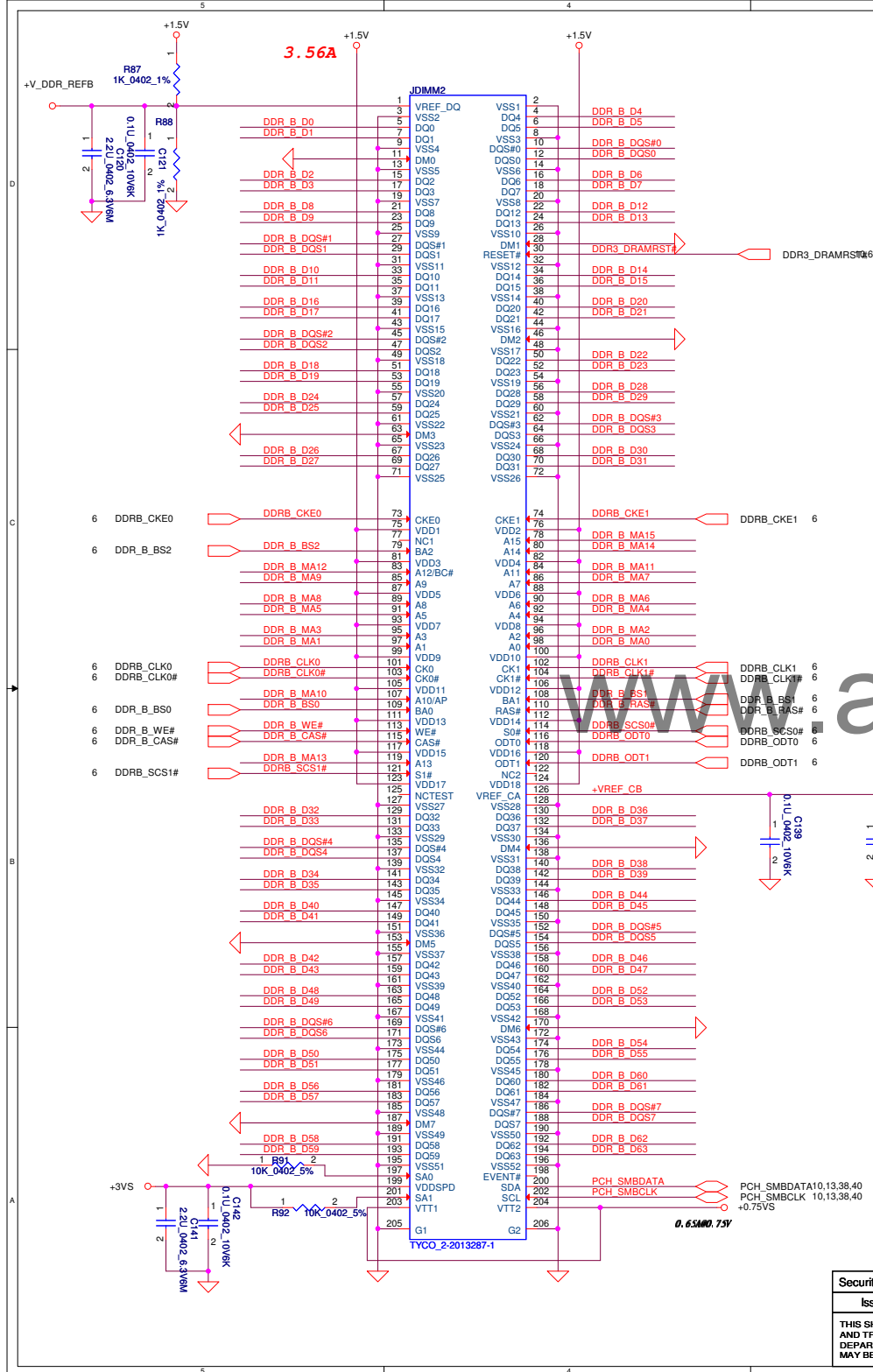


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

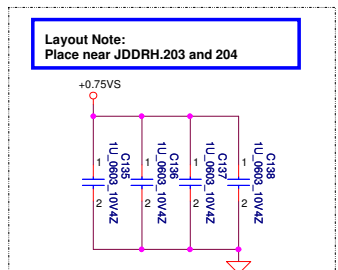
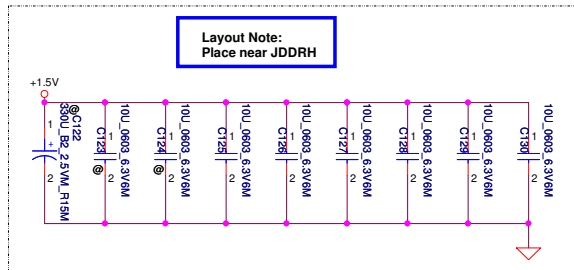
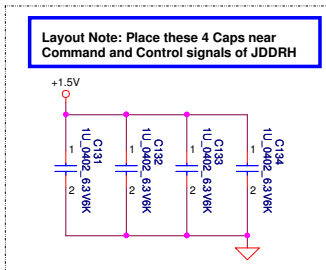


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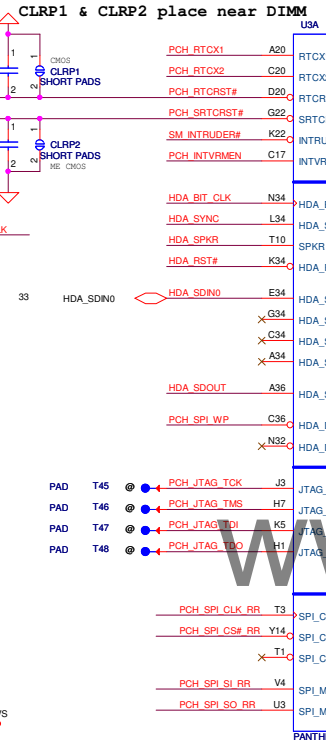
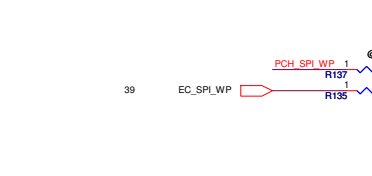
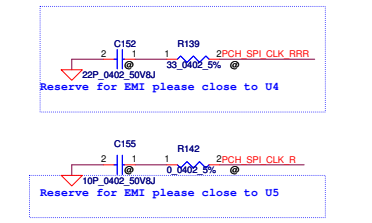
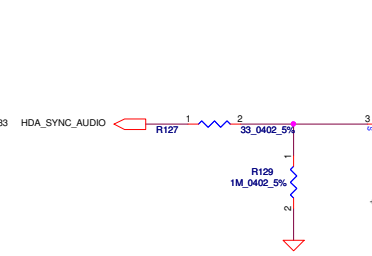
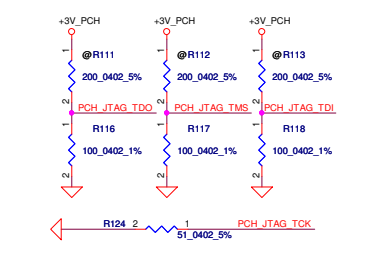
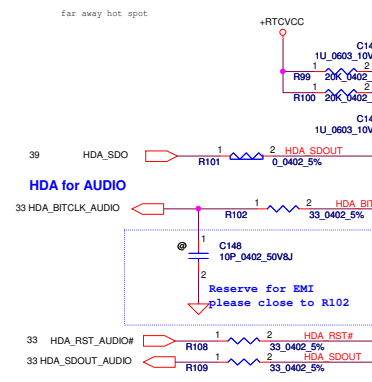
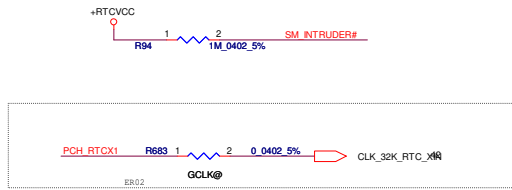
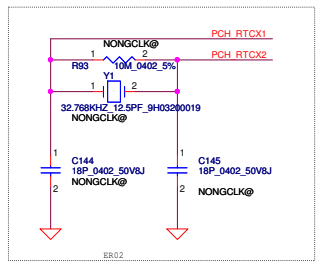




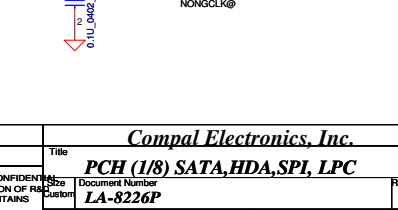
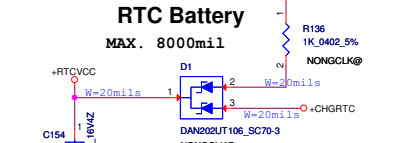
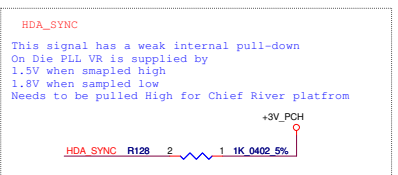
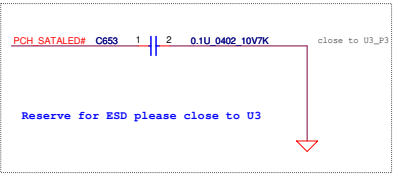
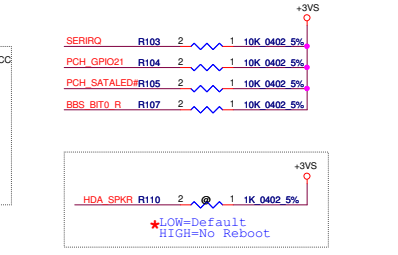
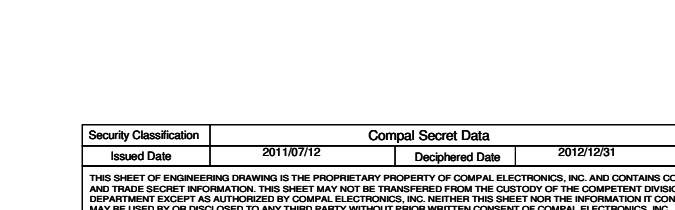
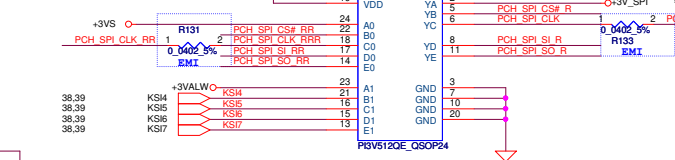
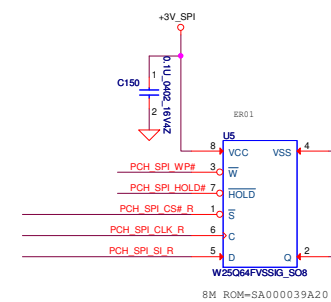
- 6 DDR_B_DQS#[0..7]
- 6 DDR_B_D[0..63]
- 6 DDR_B_DQS[0..7]
- 6 DDR_B_MA[0..15]



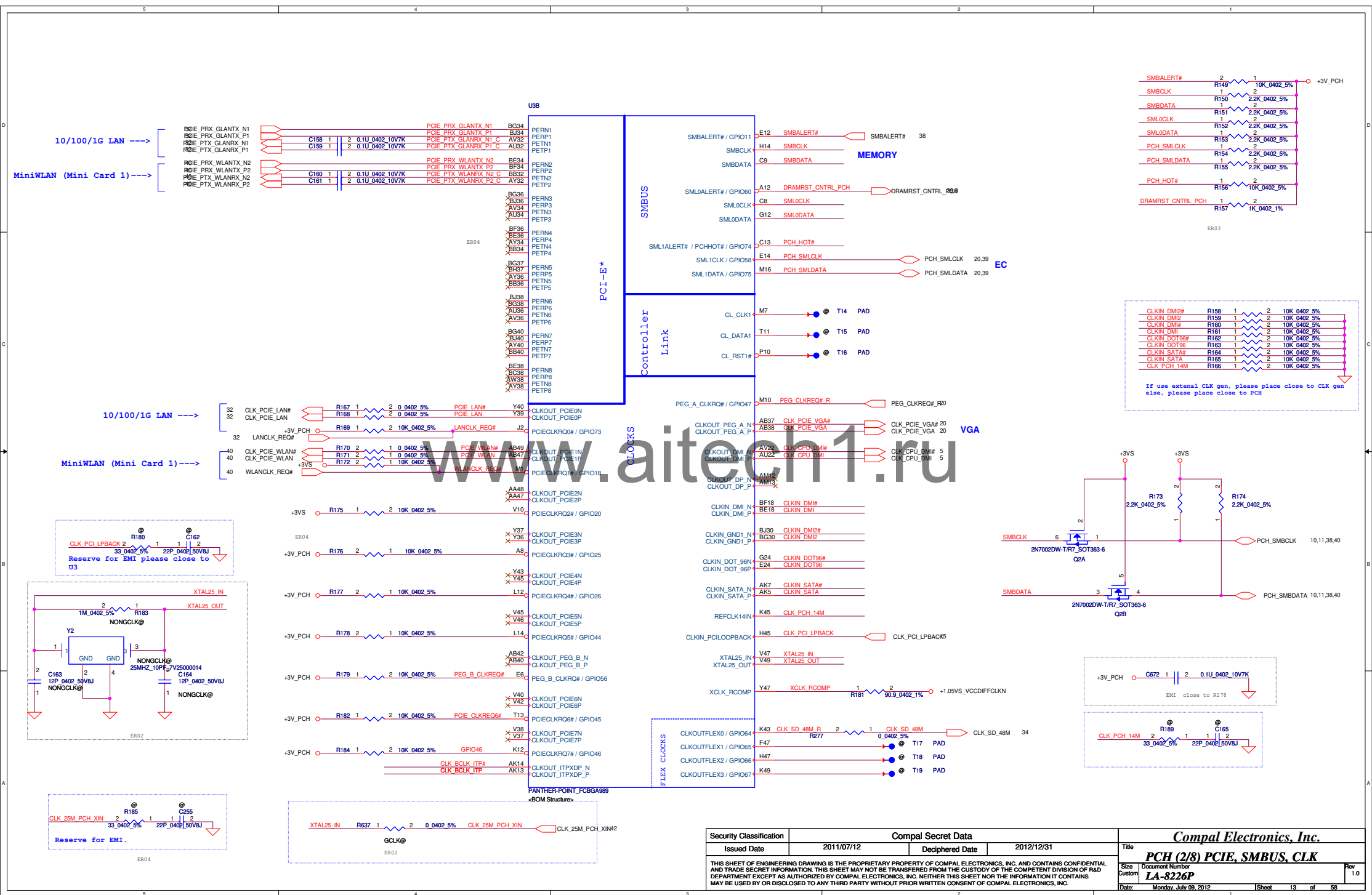
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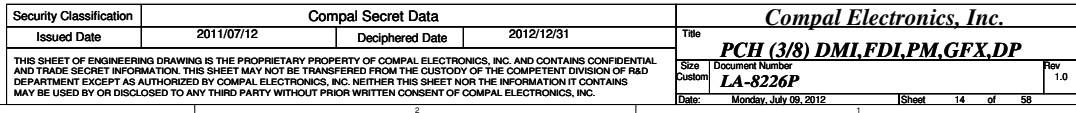


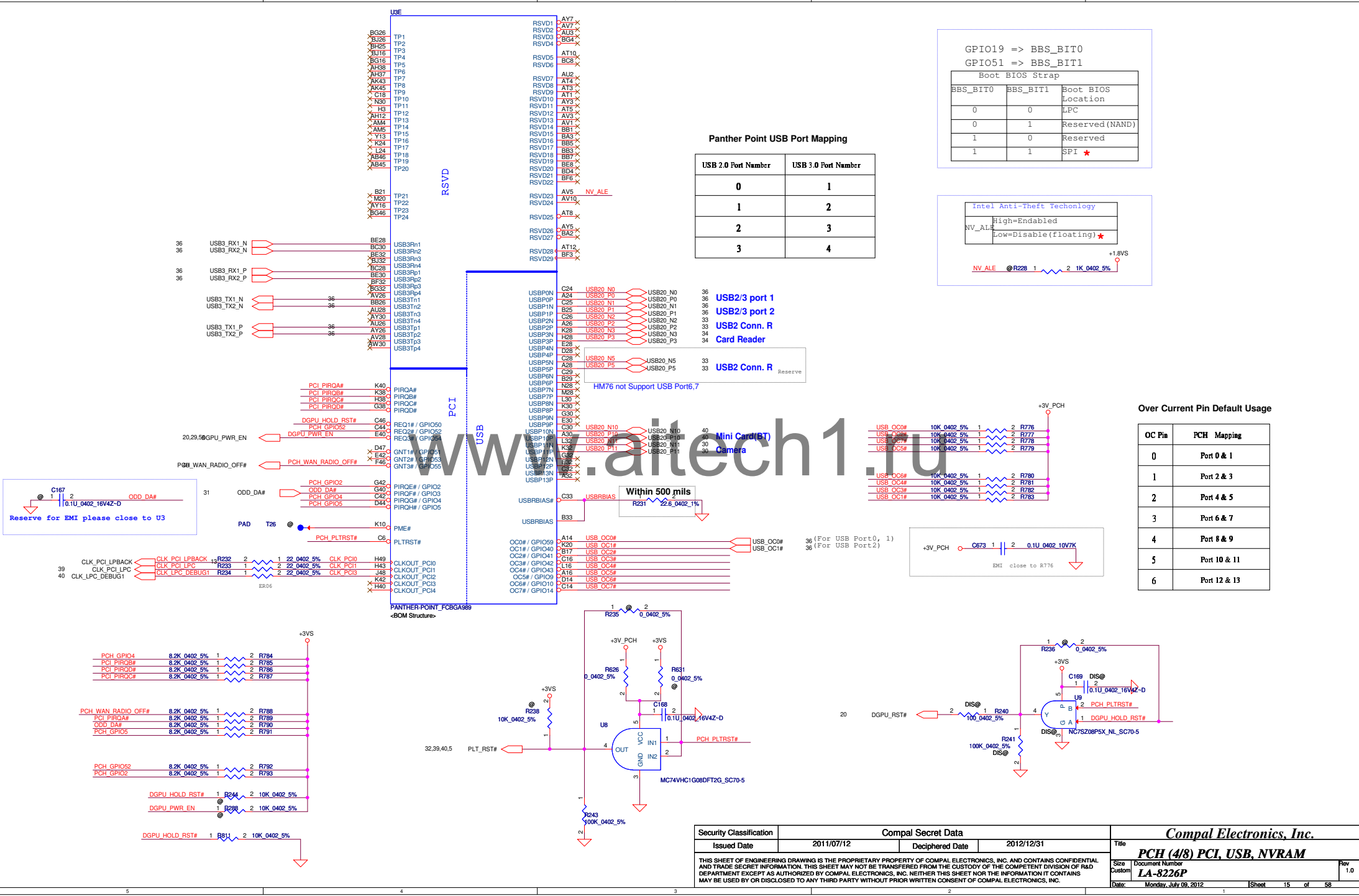
SPI ROM (8MByte)

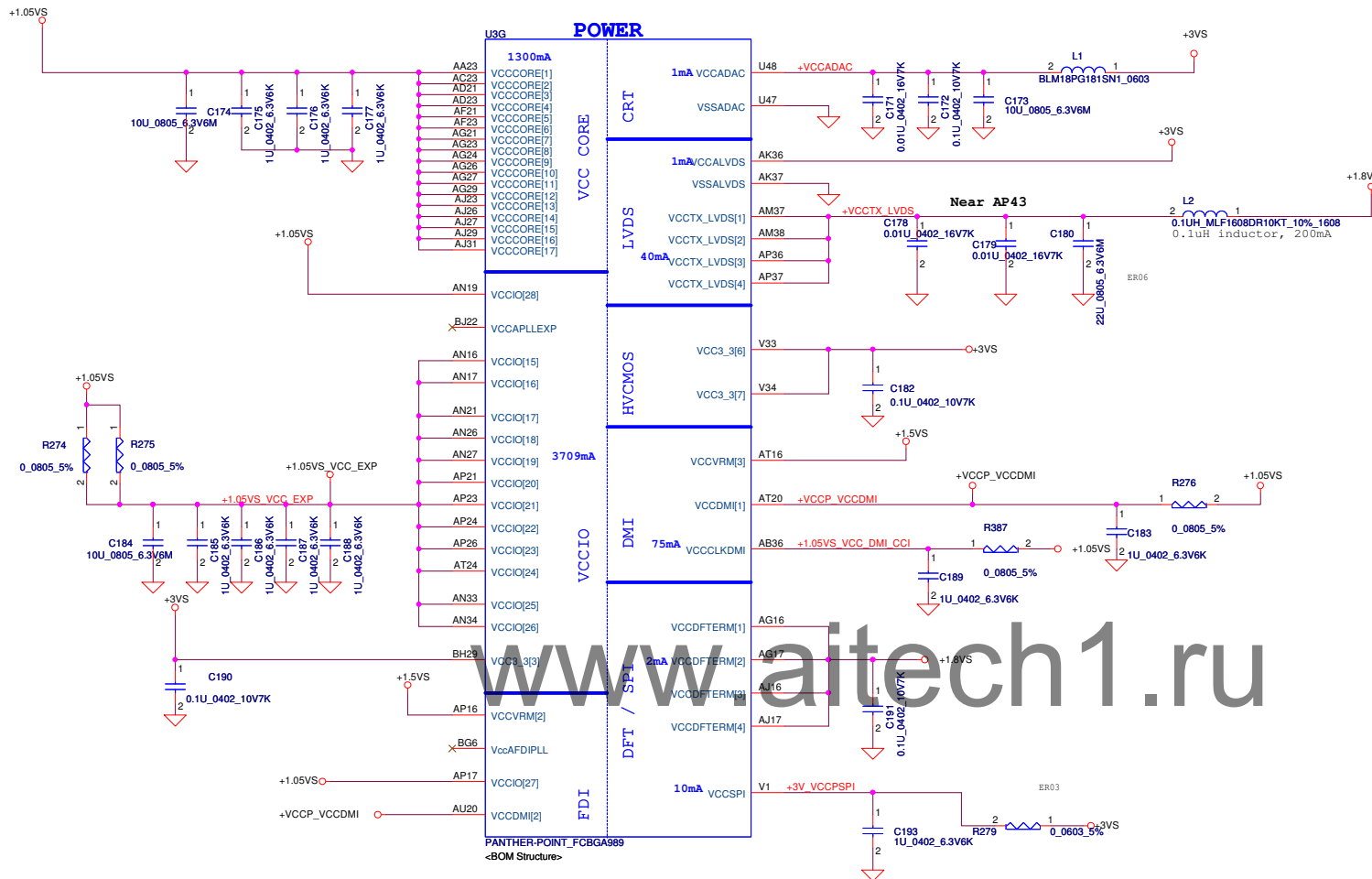


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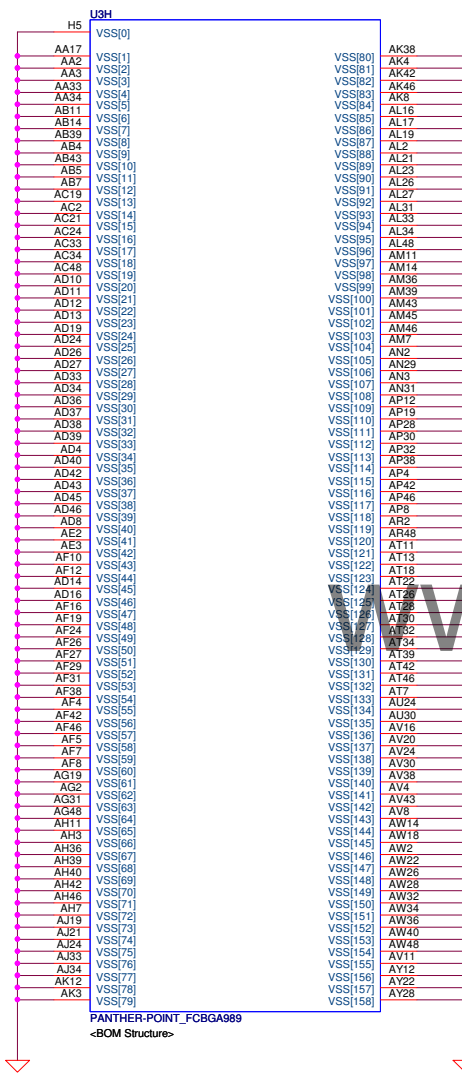








PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



PANTHER-POINT_FC8GA989

<BOM Structure>



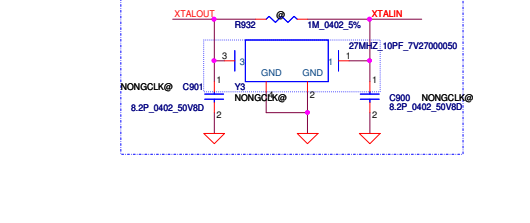
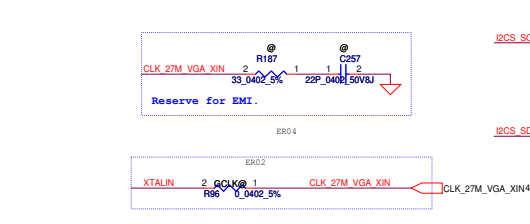
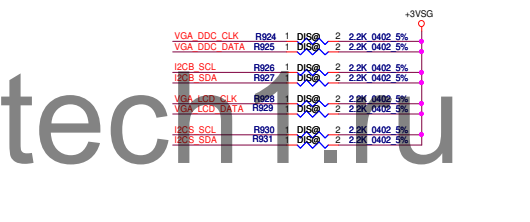
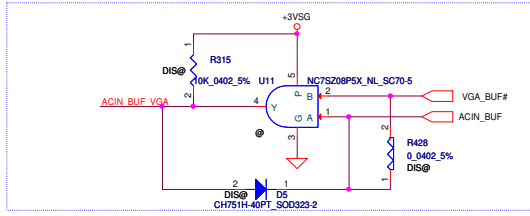
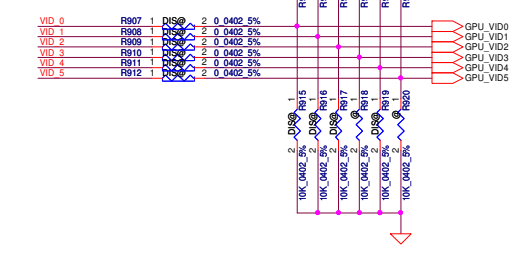
PANTHER-POINT_FC8GA989

<BOM Structure>

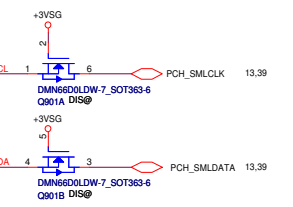
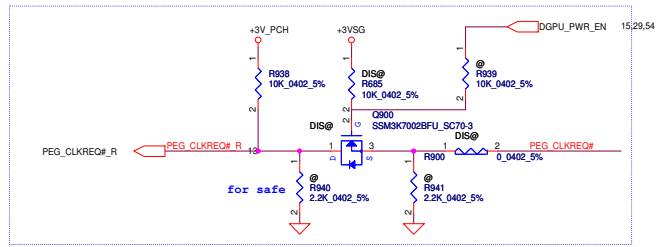
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	PCH (8/8) VSS
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PCIE GTX_C_CRX_P0_15]	PCIE GTX_C_CRX_P0_15]
PCIE GTX_C_CRX_N0_15]	PCIE GTX_C_CRX_N0_15]
PCIE GTX_C_CRX_P0_15]	PCIE GTX_C_CRX_P0_15]
PCIE GTX_C_CRX_N0_15]	PCIE GTX_C_CRX_N0_15]

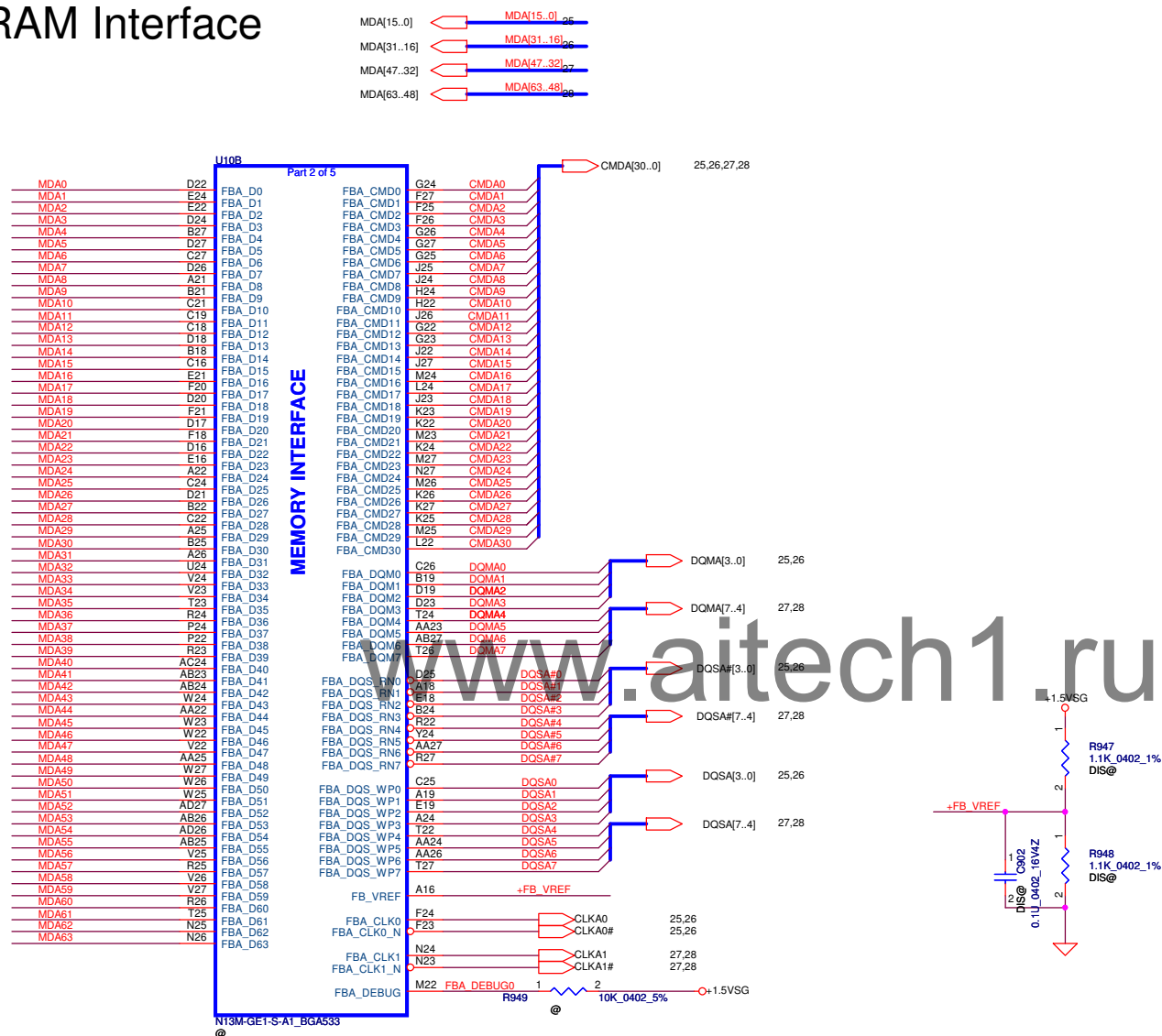
for GS4, the boot voltage is 0.975V
for GV4, the boot voltage is 0.85V



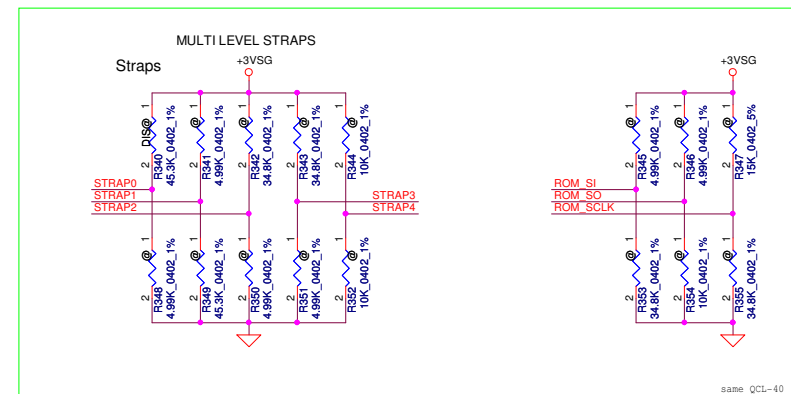
GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VDD
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D_Vision
GPIO8	I/O	OVERT#
GPIO9	I/O	ALERT#
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU_VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved



VRAM Interface

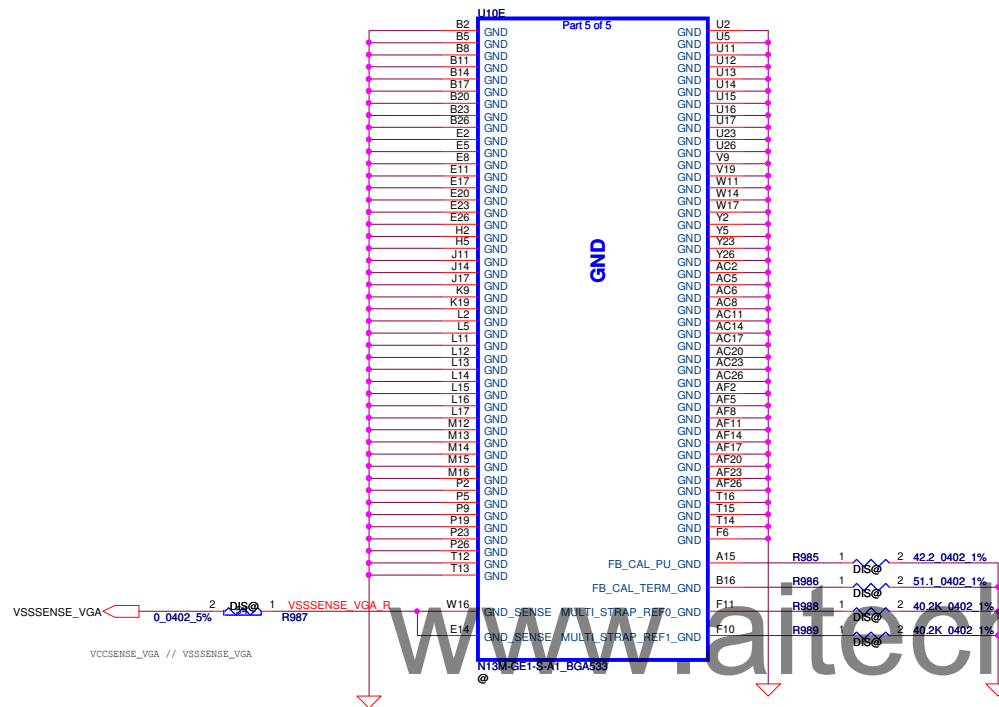


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				Date:	Monday, July 09, 2012	Sheet 21 of 58



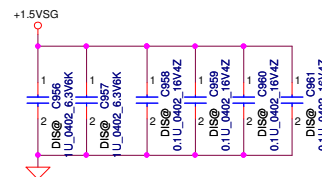
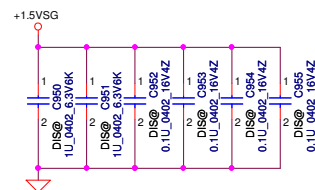
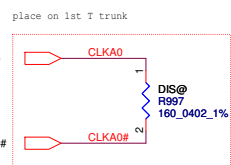
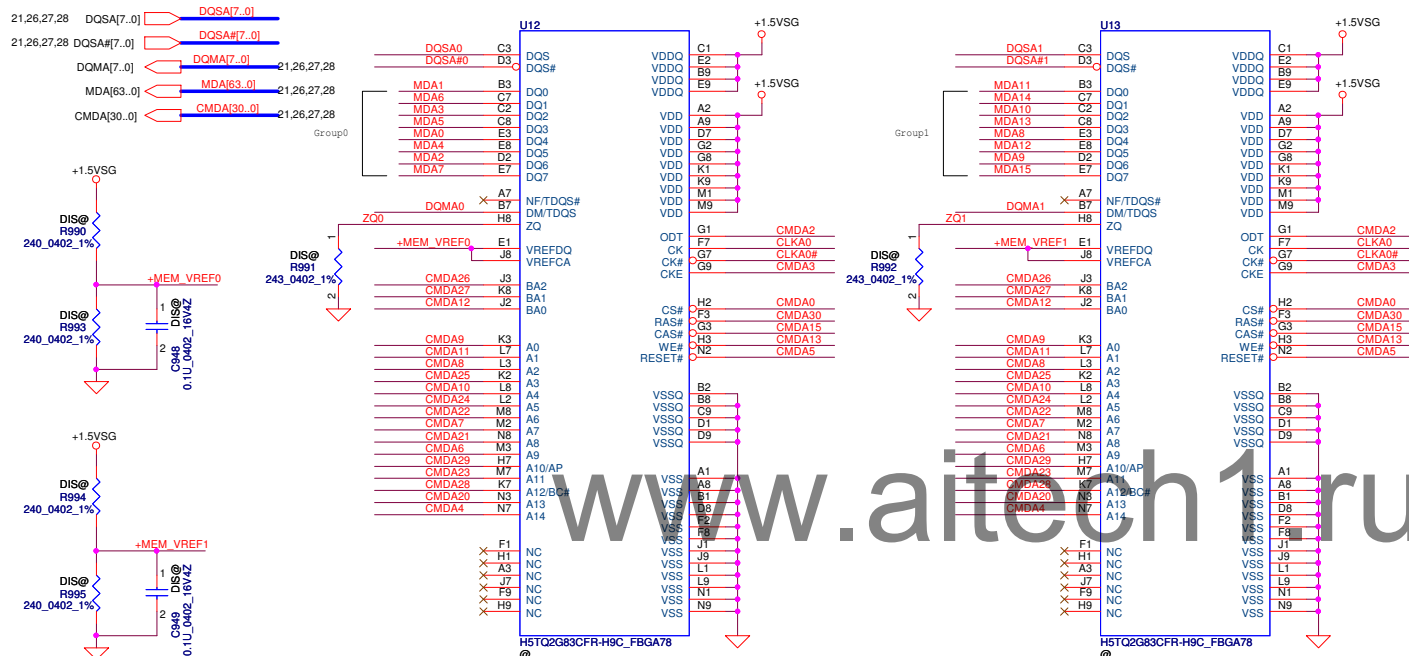
	GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_S1	ROM_S0	ROM_SCLK
1	N13M-S02	800 MHz	256M* 8* 8 2GB	ELPIDA SA000056P00 ED12108CSE-DJ-F	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PU 10K	R PU 5K
07	N13M-S02	800 MHz	256M* 8* 8 2GB	HYNIX SA000056P00 H57QX2G83CFF-H9C	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PU 10K	R PU 5K

256M*8*8
1.SA000056000
DDR3 1600 256*8 1.5V FBGA78
HYNIX/H5TQ2G83CFR-PBC
2.SA000056P00
DDR3 1600 256*8 1.5V FBGA78
ELPIDA/EDJ2108BDBG-GN-F



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256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

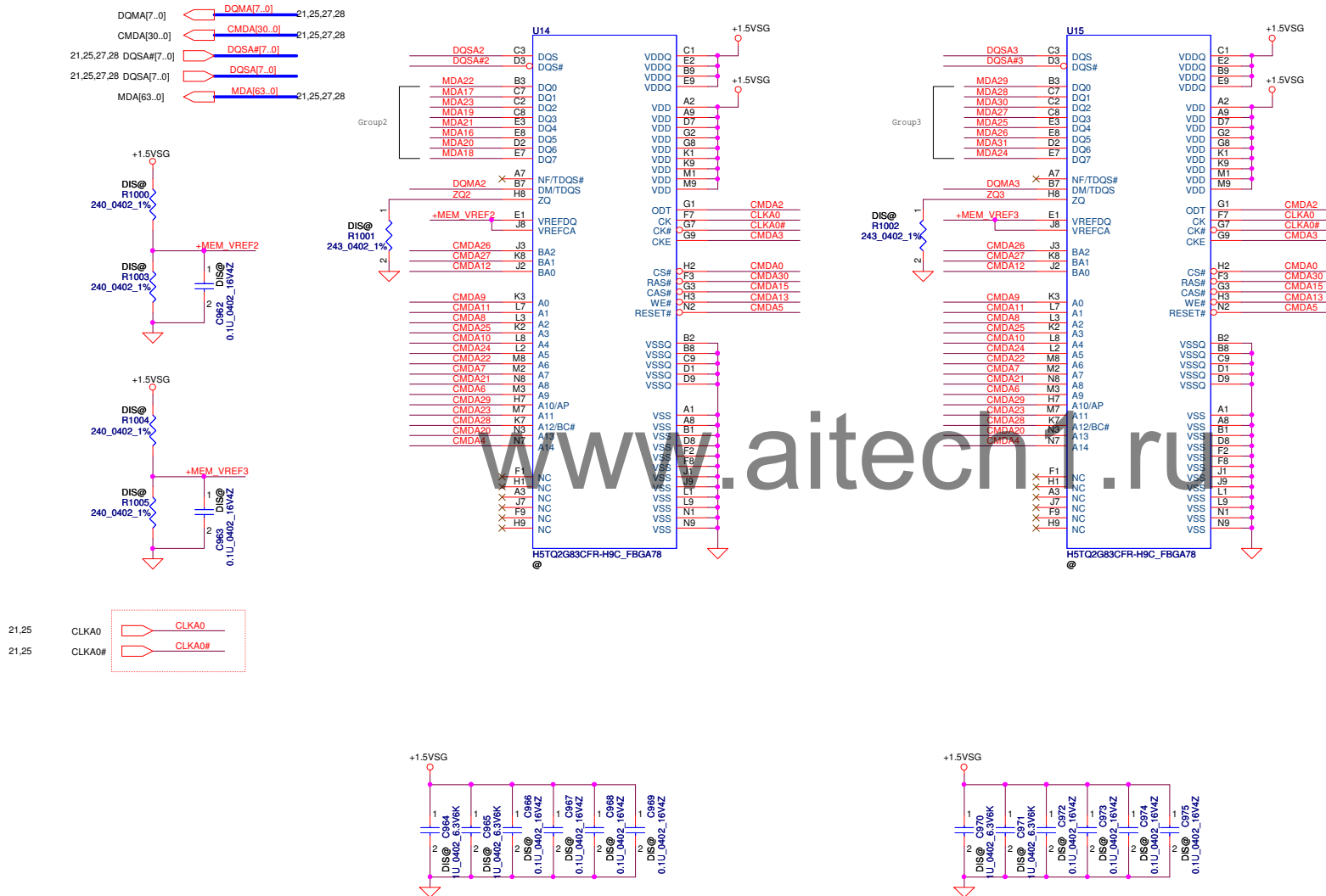
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)

Elpida : SAxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

VRAM DDR3 chips

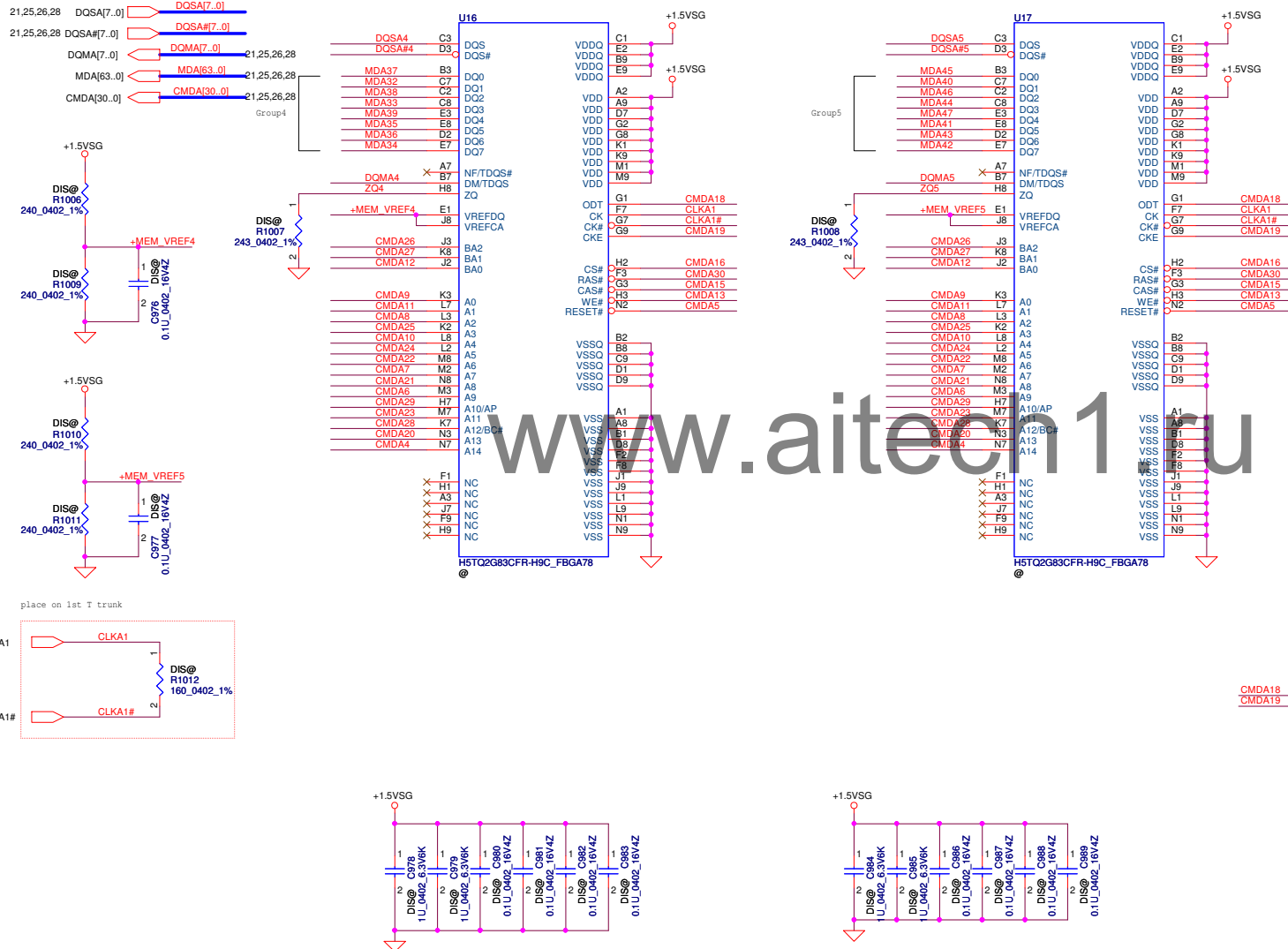
256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB

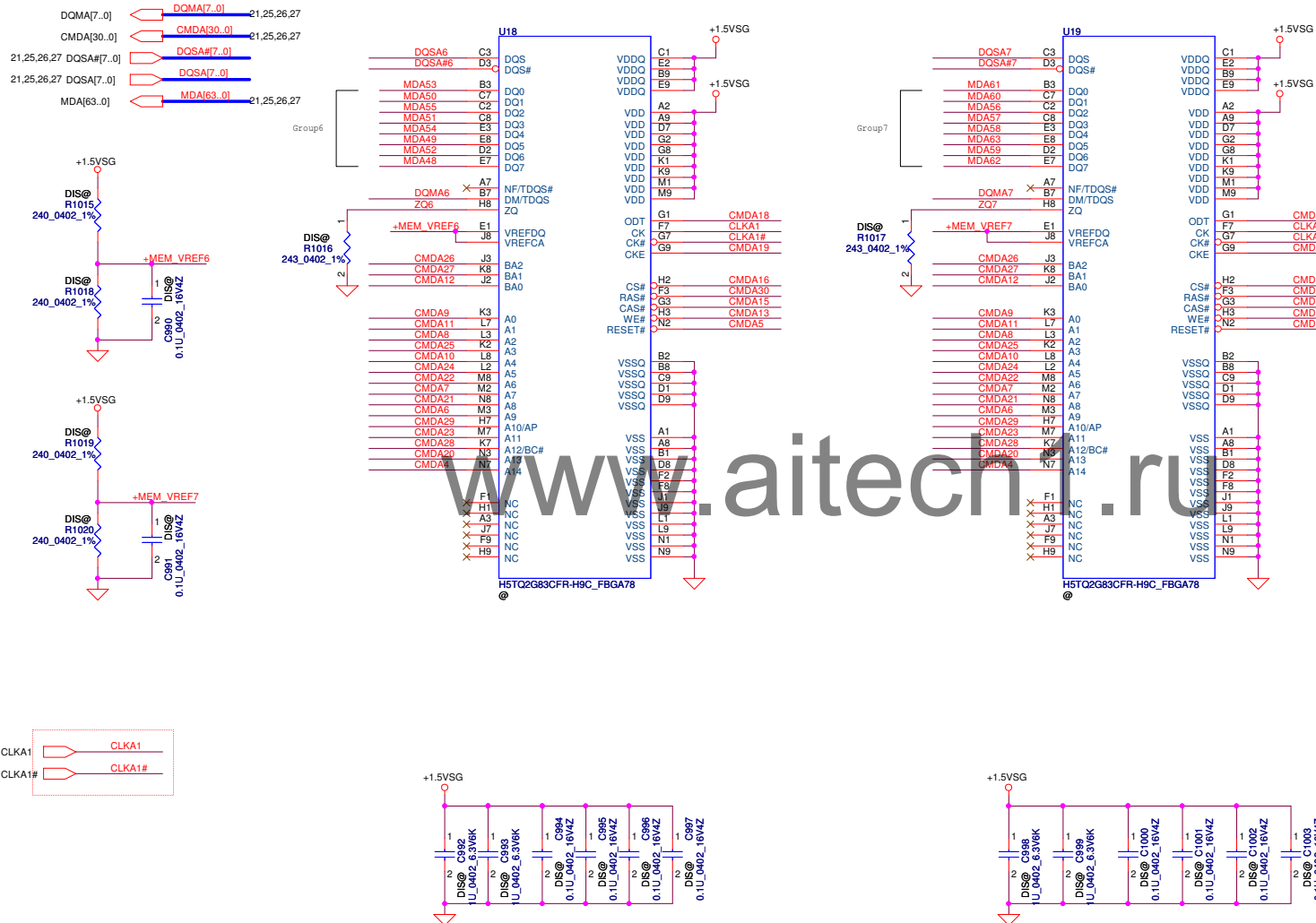


Mode	D Address	0..31	32..63
CMD0	CS0_L#		
CMD1			
CMD2	ODT_L		
CMD3	CKE		
CMD4	A14	A14	
CMD5	RST	RST	
CMD6	A9	A9	
CMD7	A7	A7	
CMD8	A2	A2	
CMD9	A0	A0	
CMD10	A4	A4	
CMD11	A1	A1	
CMD12	BA0	BA0	
CMD13	WE*	WE*	
CMD14	A15	A15	
CMD15	CAS*	CAS*	
CMD16		CS0_H#	
CMD17			
CMD18		ODT_H	
CMD19		CKE_H	
CMD20	A13	A13	
CMD21	A8	A8	
CMD22	A6	A6	
CMD23	A11	A11	
CMD24	A5	A5	
CMD25	A3	A3	
CMD26	BA2	BA2	
CMD27	BA1	BA1	
CMD28	A12	A12	
CMD29	A10	A10	
CMD30	RAS*	RAS*	
Not Available		LOW	HIGH

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

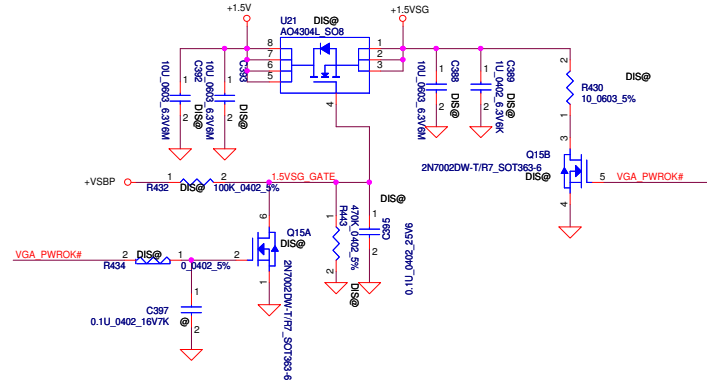
VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB

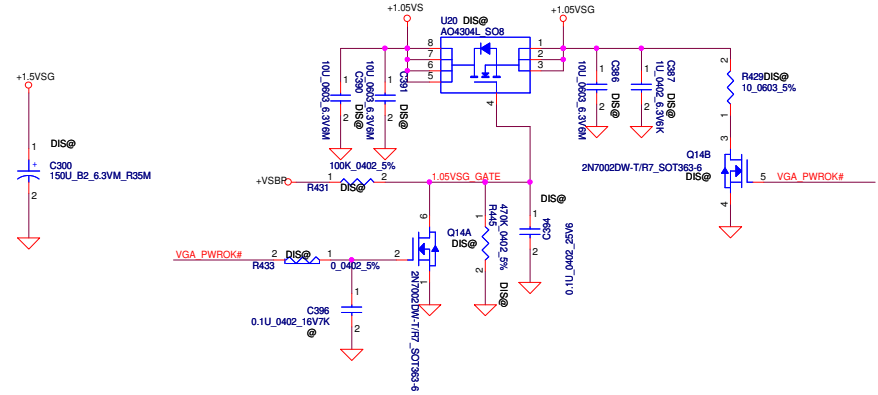


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
LOW		HIGH

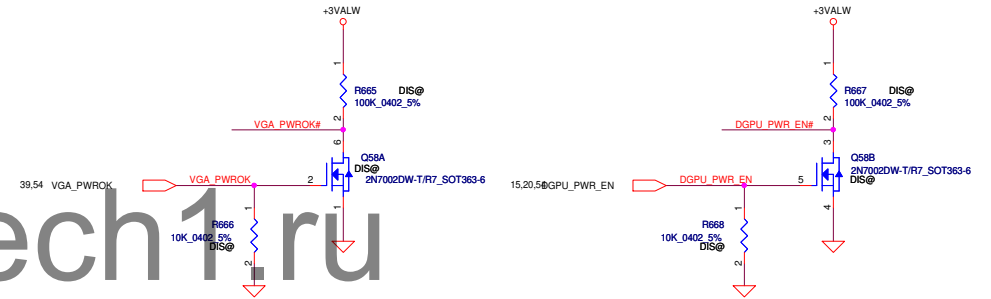
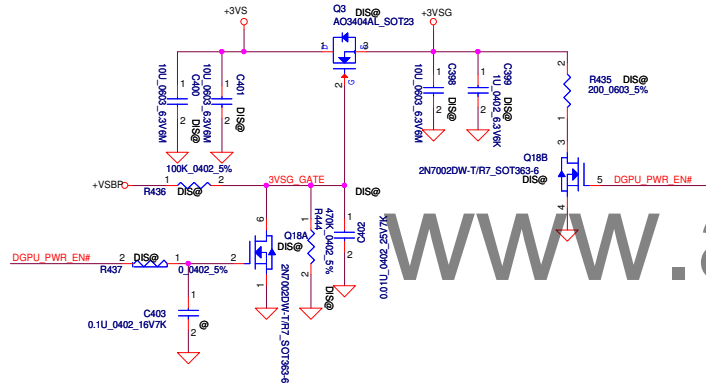
+1.5V to +1.5VSG



+VCCP to +1.05VSG

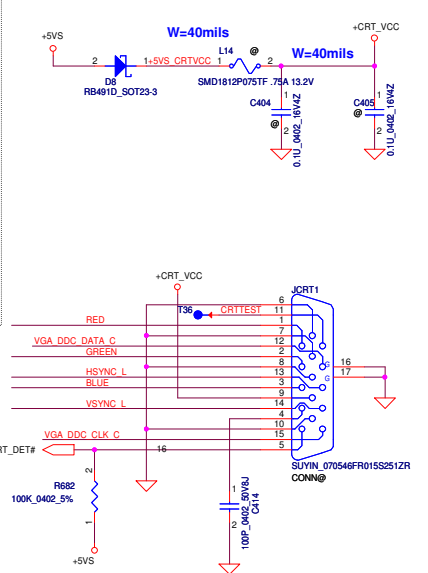
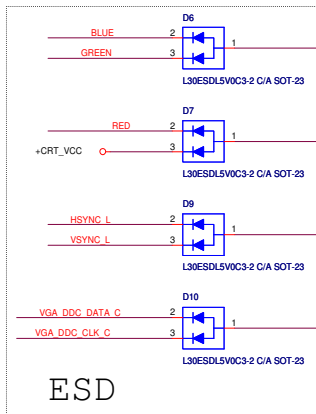


+3VS to +3VSG



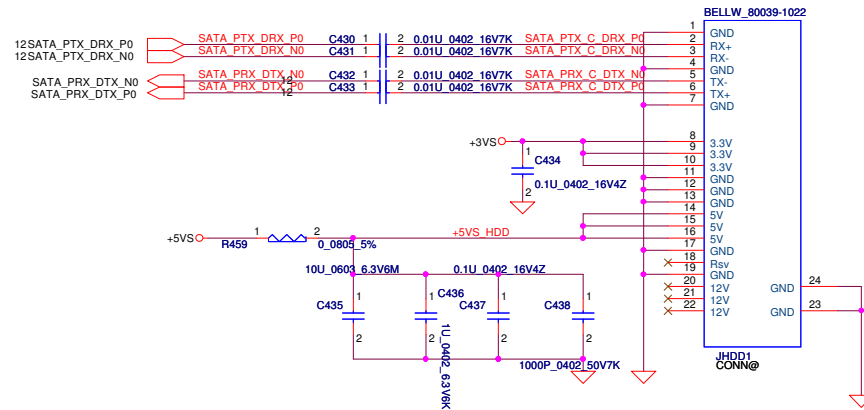
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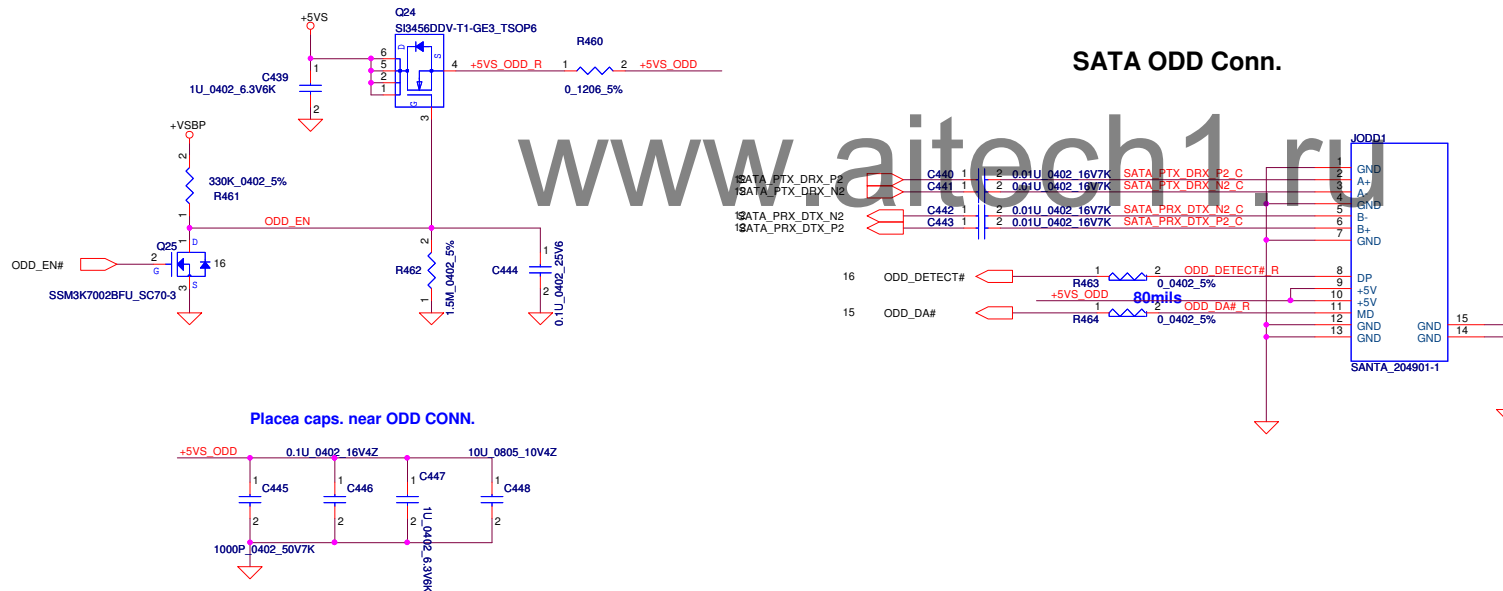


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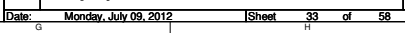
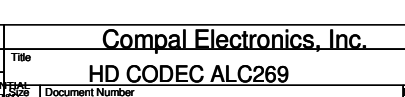
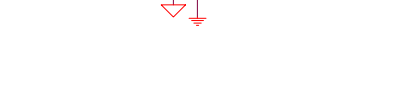
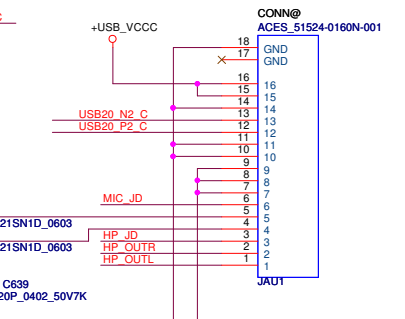
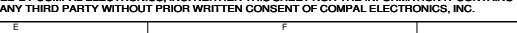
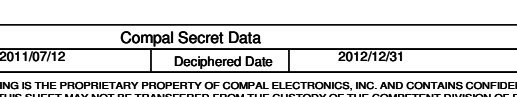
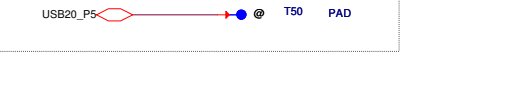
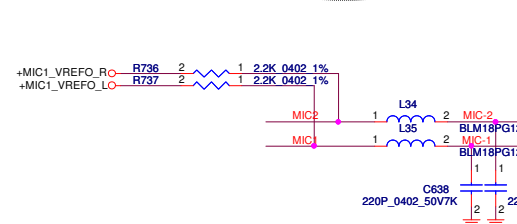
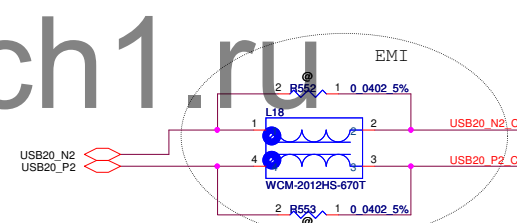
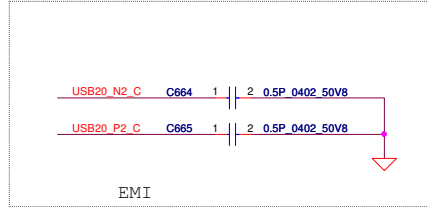
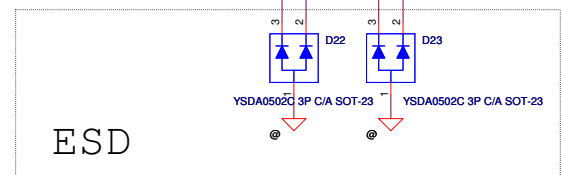
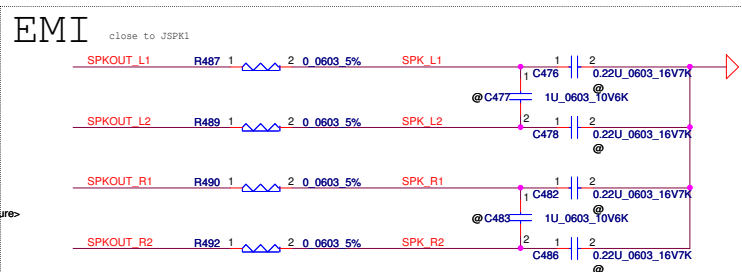
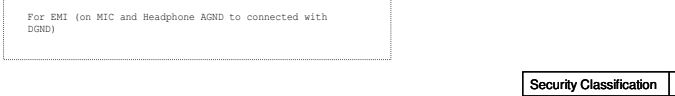
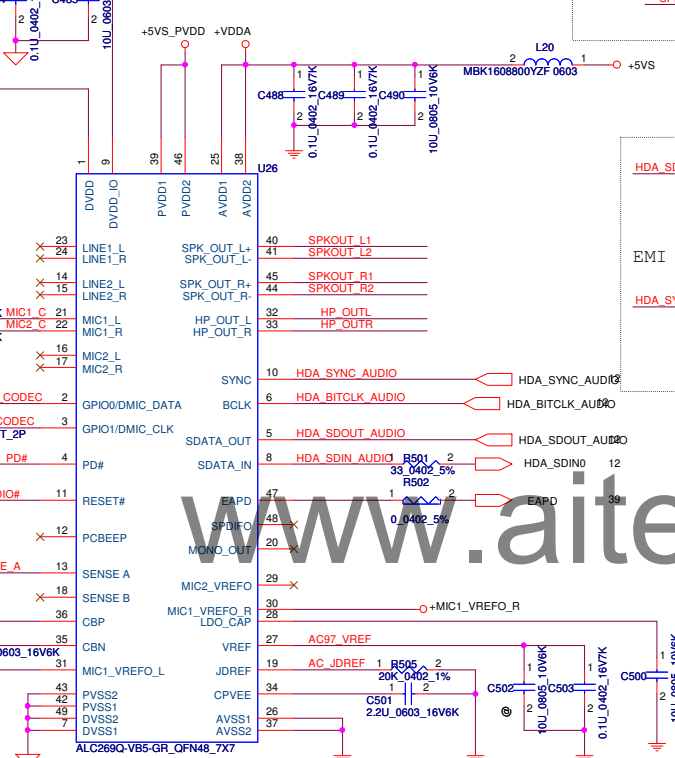
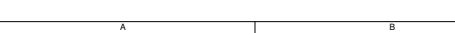
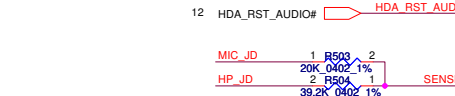
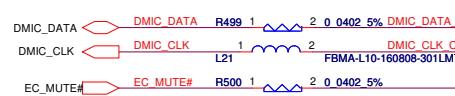
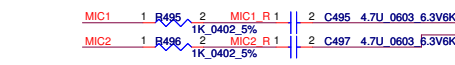
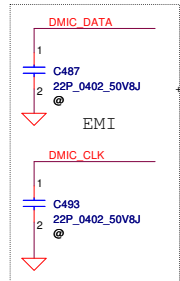
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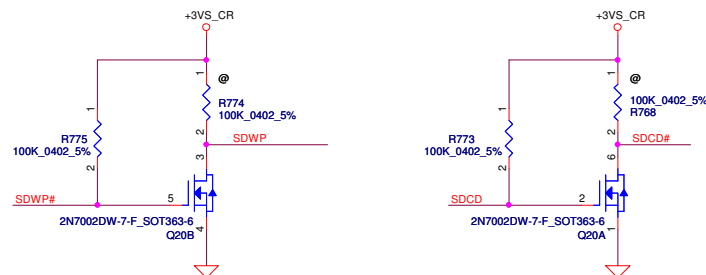
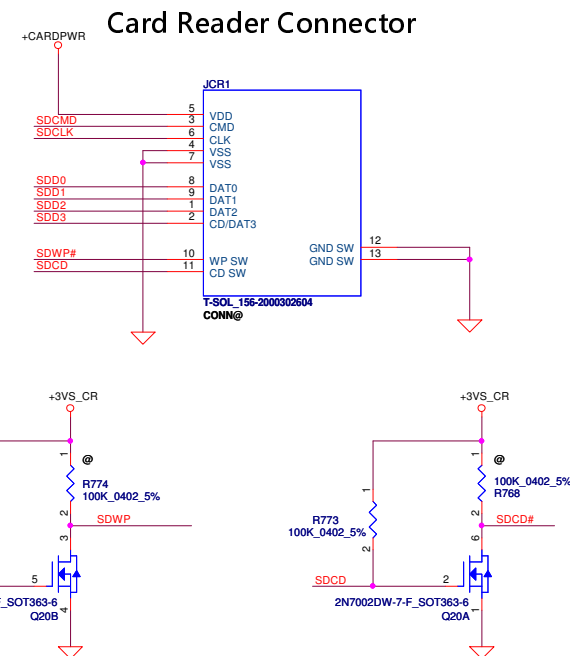
SATA ODD Conn.



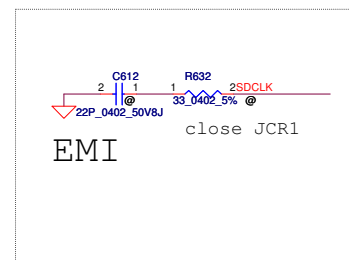
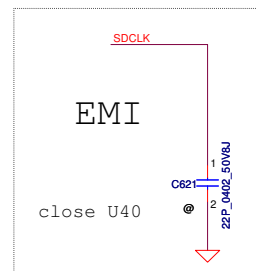
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				Document Number	Rev
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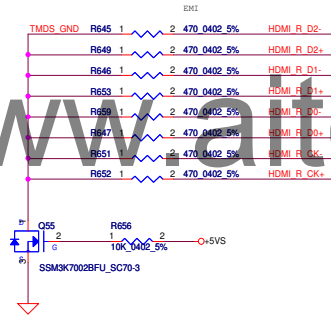
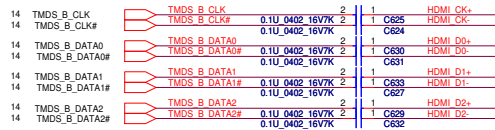
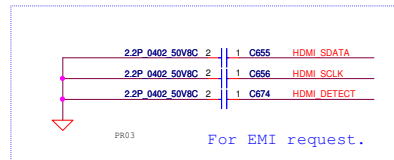
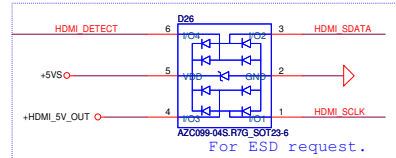
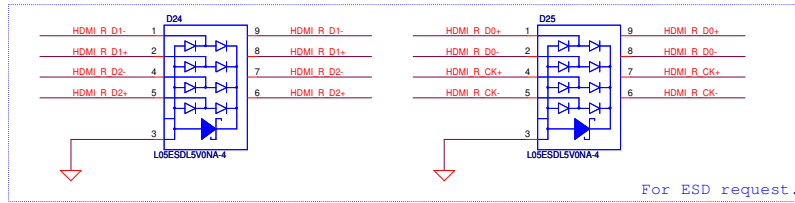


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				Sheet	33 of 58

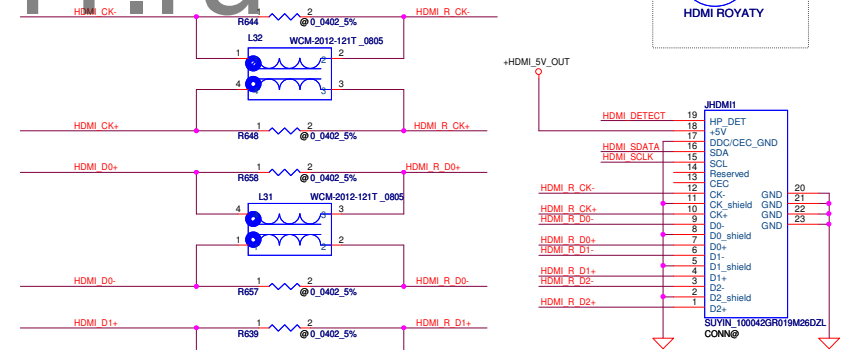
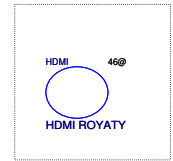
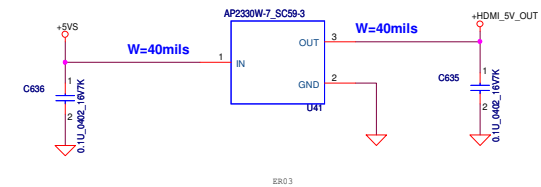
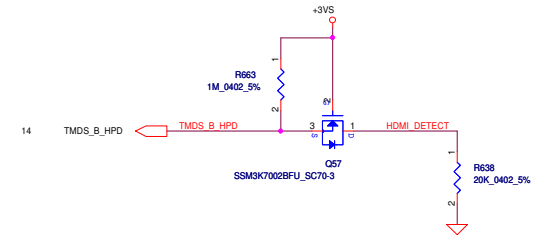
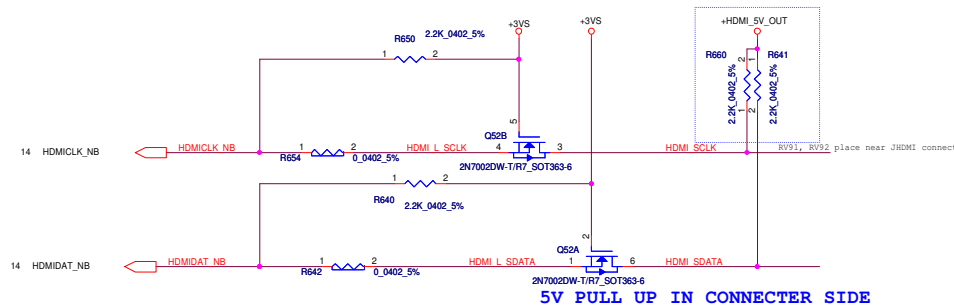


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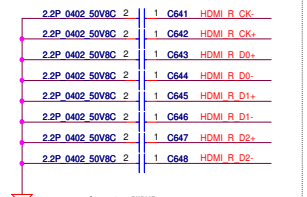




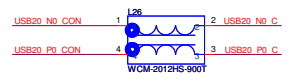
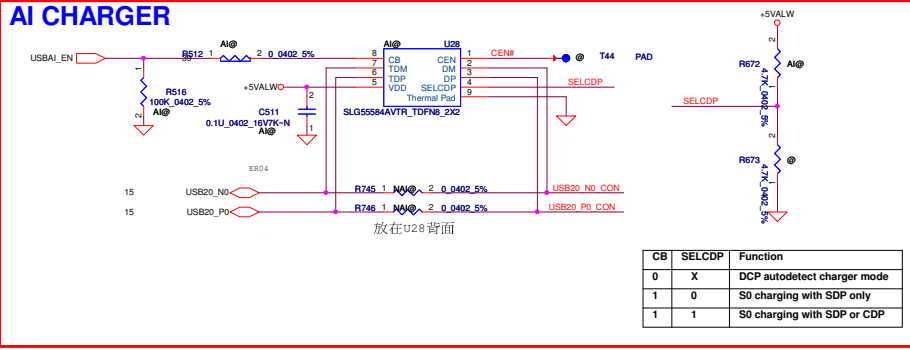
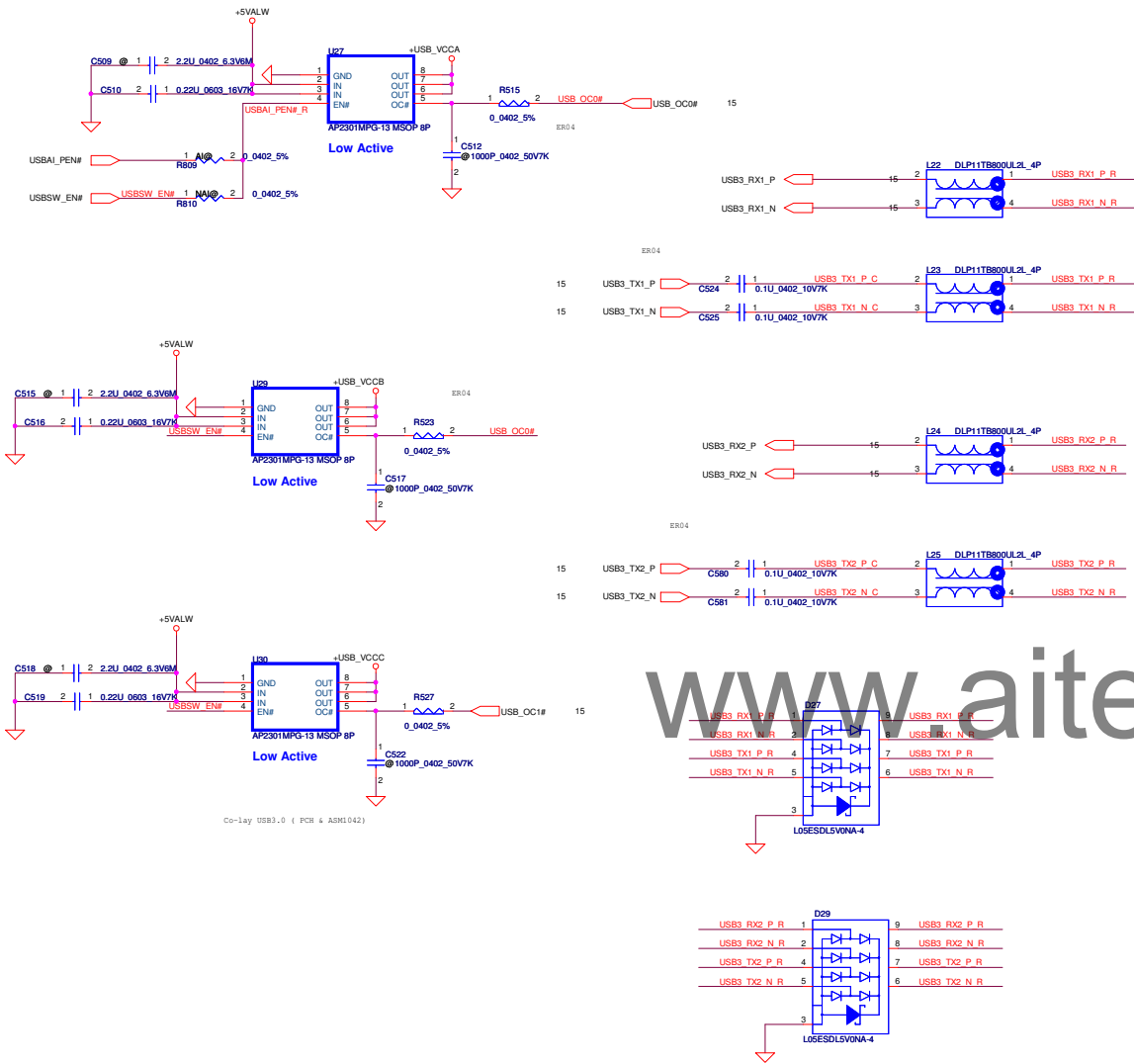
HDMI



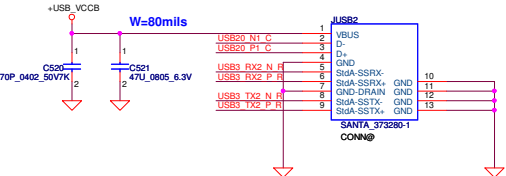
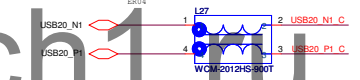
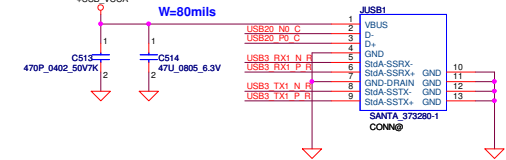
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2011/07/12		2012/12/31		Document Number	
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Date:		Monday, July 09, 2012		Sheet	
		35		of	
				58	



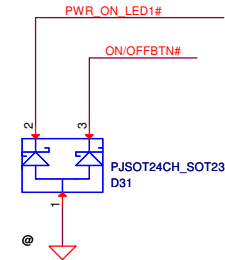
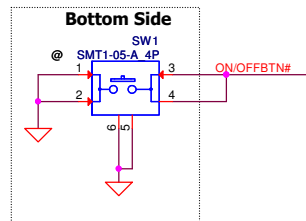
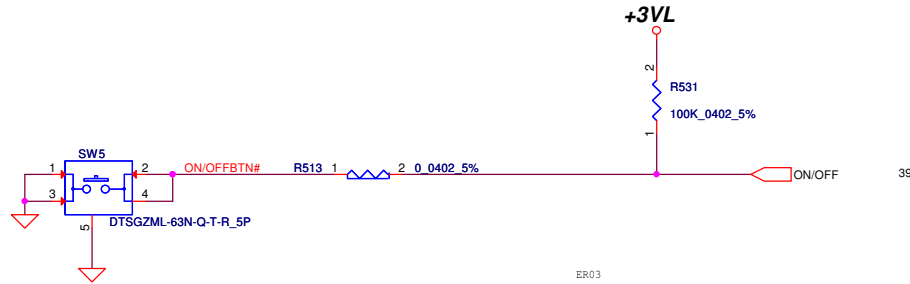
charger port: left side & near user



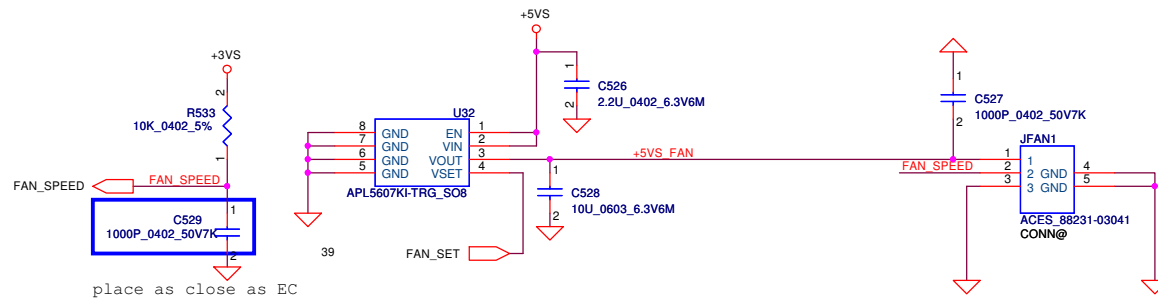
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Power Button

ON/OFF switch



Fan Control Circuit

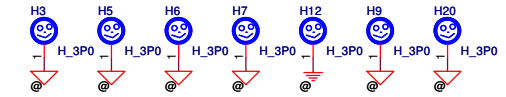


Screw Hole

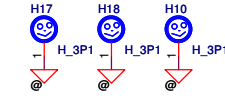
2.7



3.0



3.1



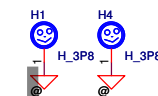
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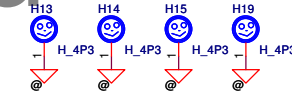
3.8



3.8

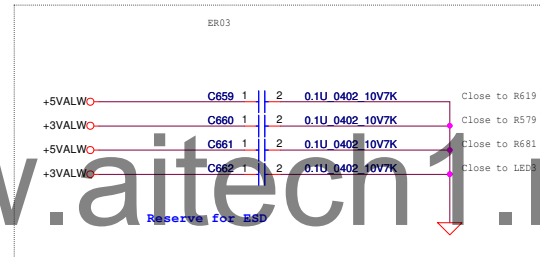
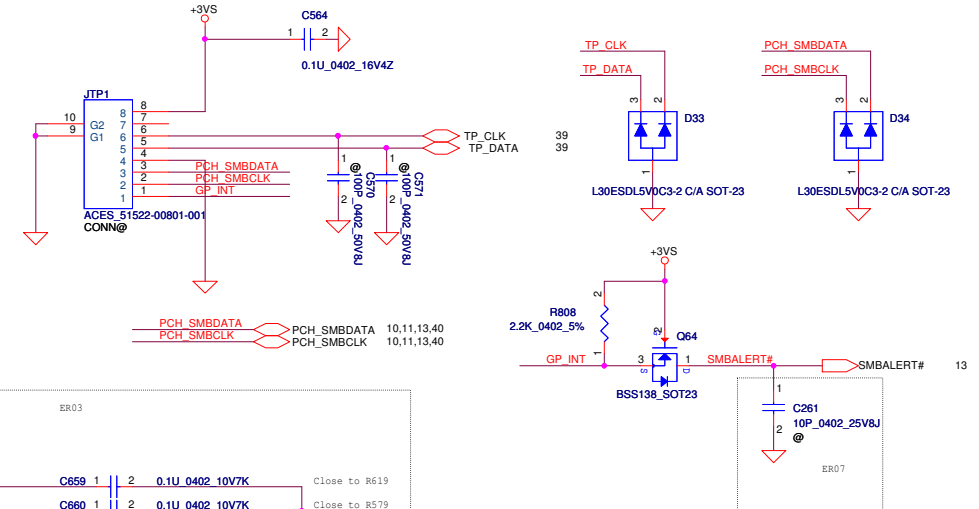
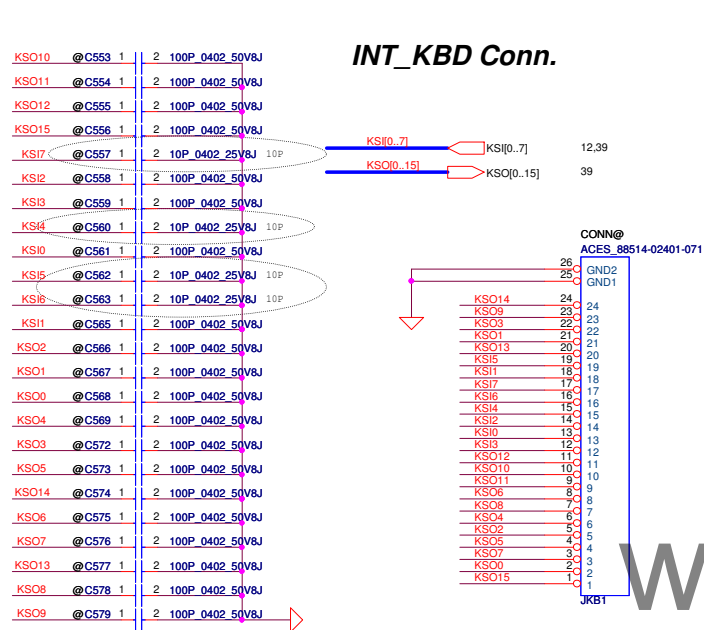


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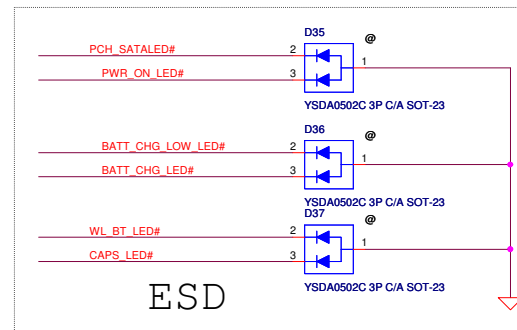
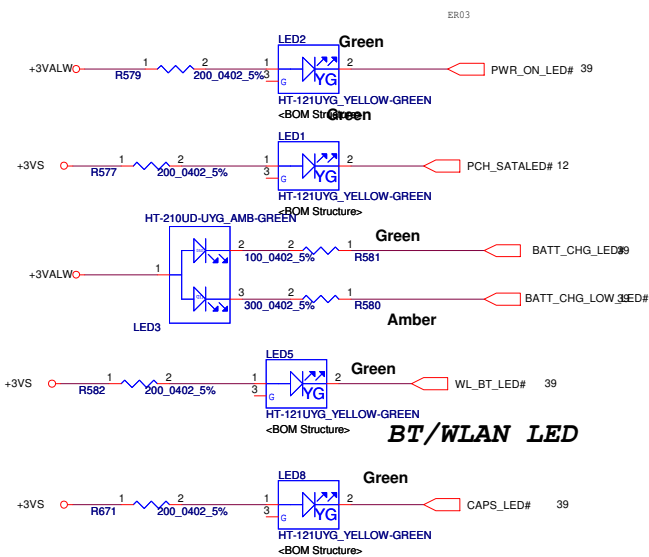


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	PWRBTN/ FAN / Screws	
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				Custom	LA-8226P	
				Date:	Monday, July 09, 2012	Sheet

Touch/B Connector

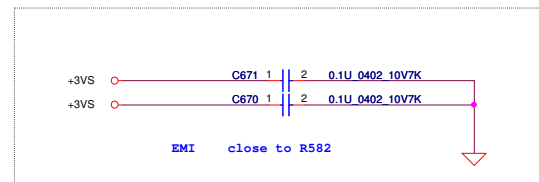
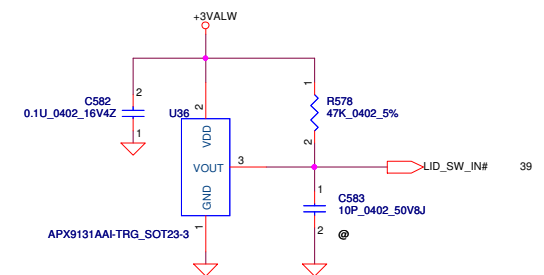


LED

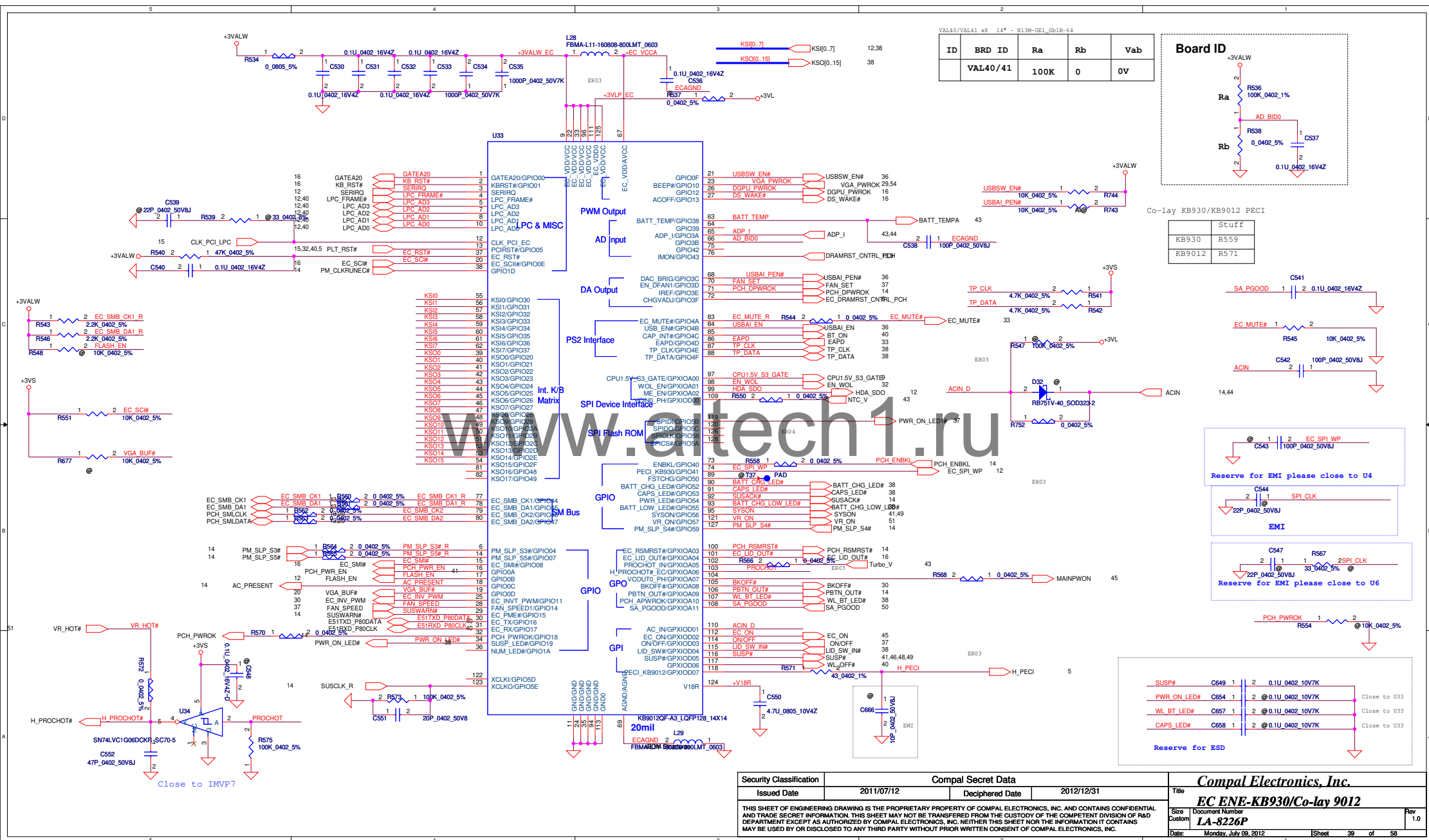


Lid Switch

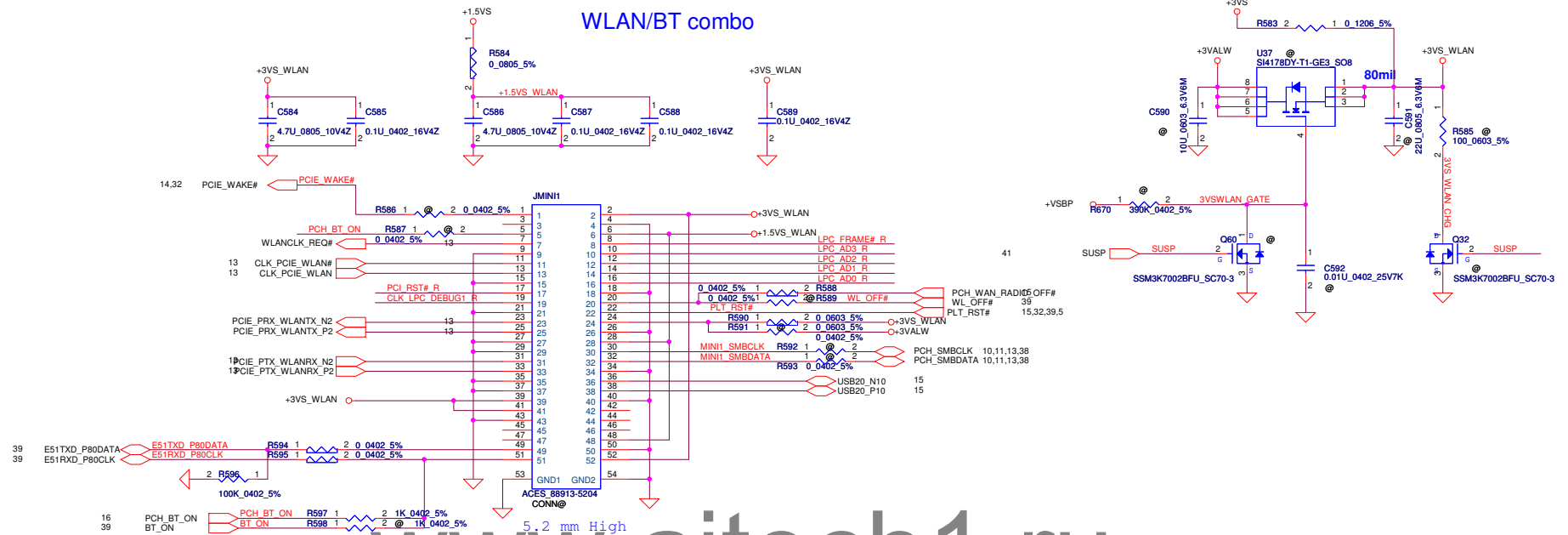
(Hall Effect Switch)



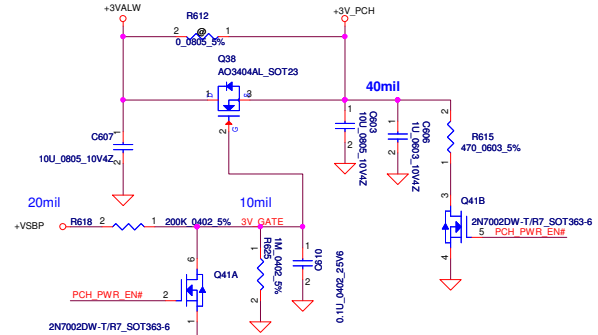
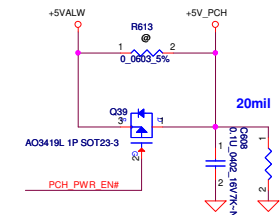
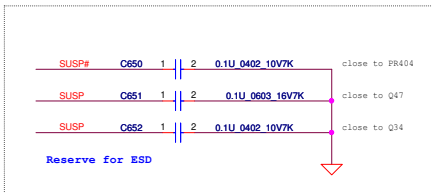
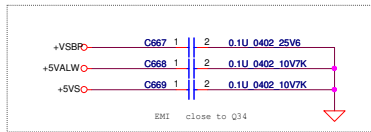
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	KB/EC ROM/TP/FUN/LED	
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				LA-8226P	1.0	
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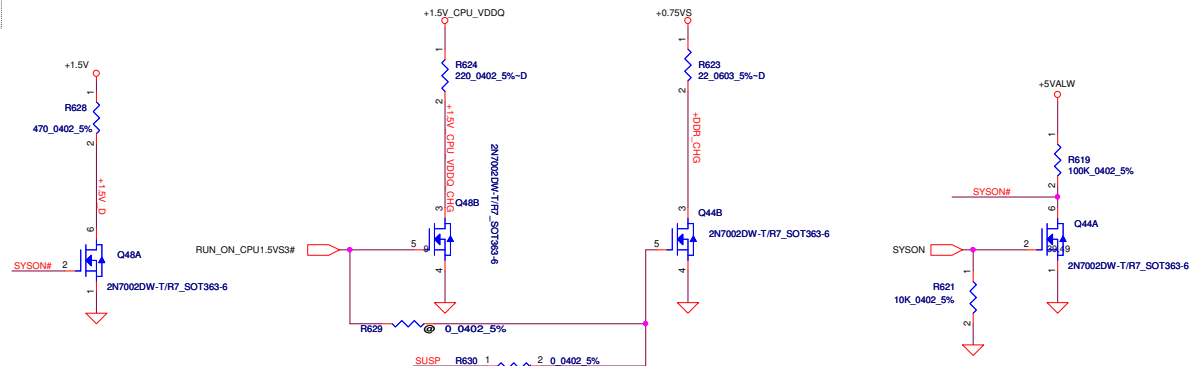
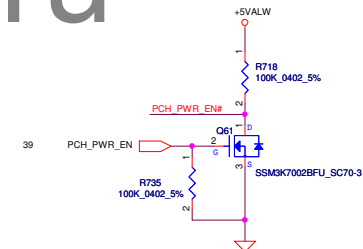
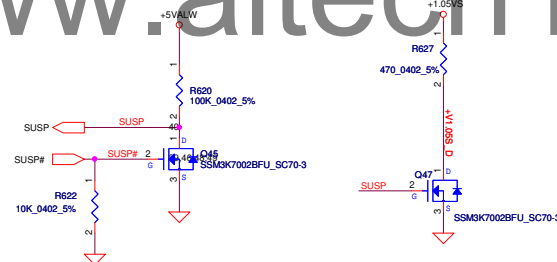
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	EC ENE-KB930/Co-lay 9012 LA-8226P
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				Monday, July 09, 2012	1.0
				Sheet 39 of 58	



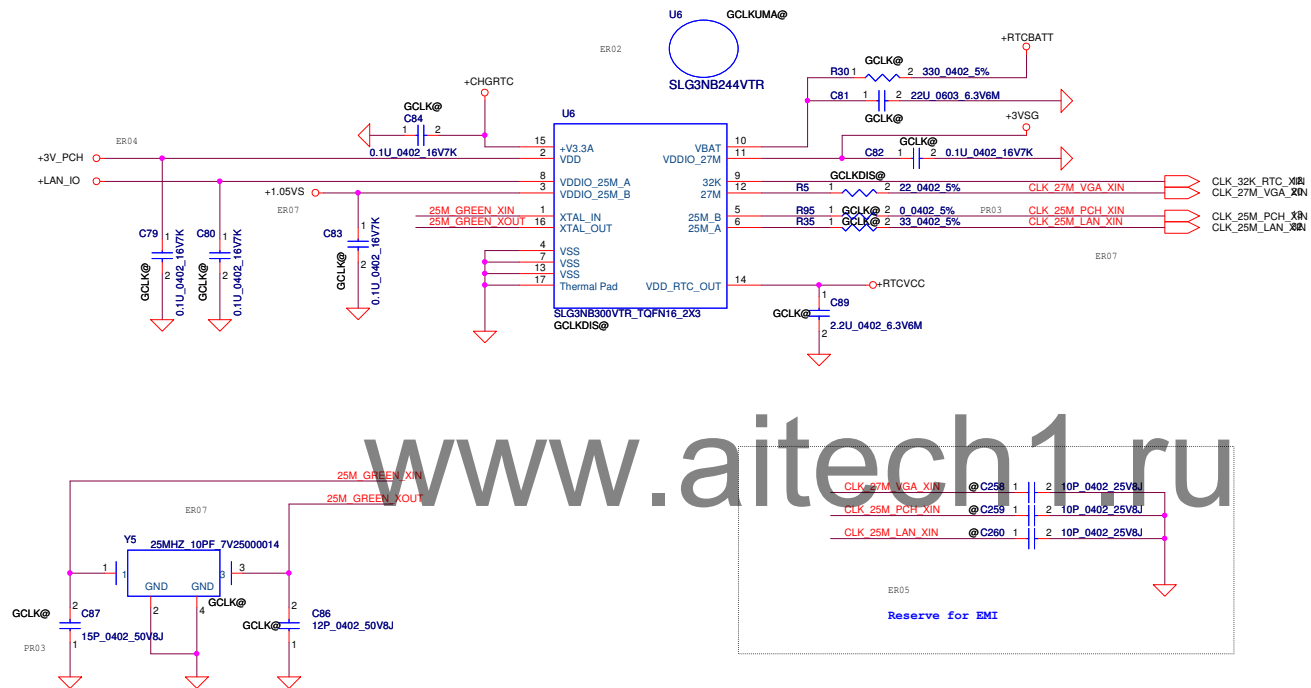
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	WLAN/ WWAN/ m-SATA
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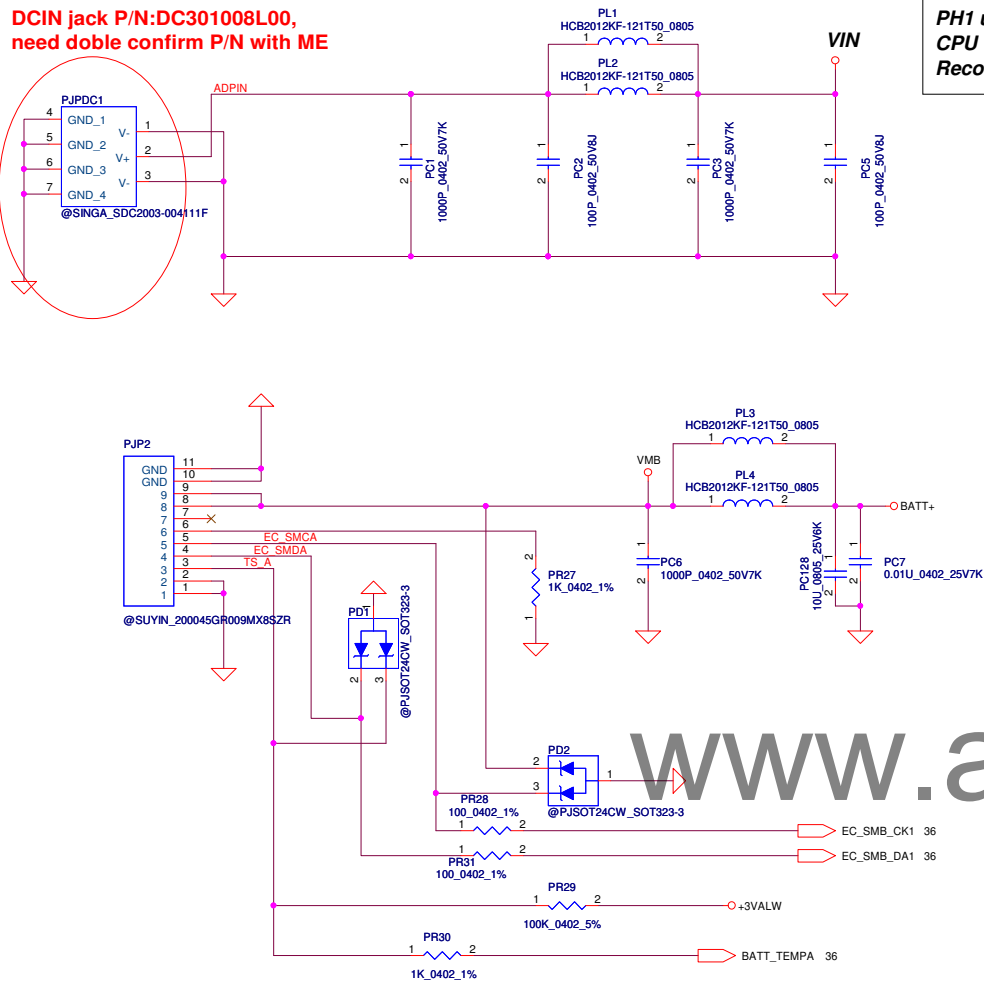


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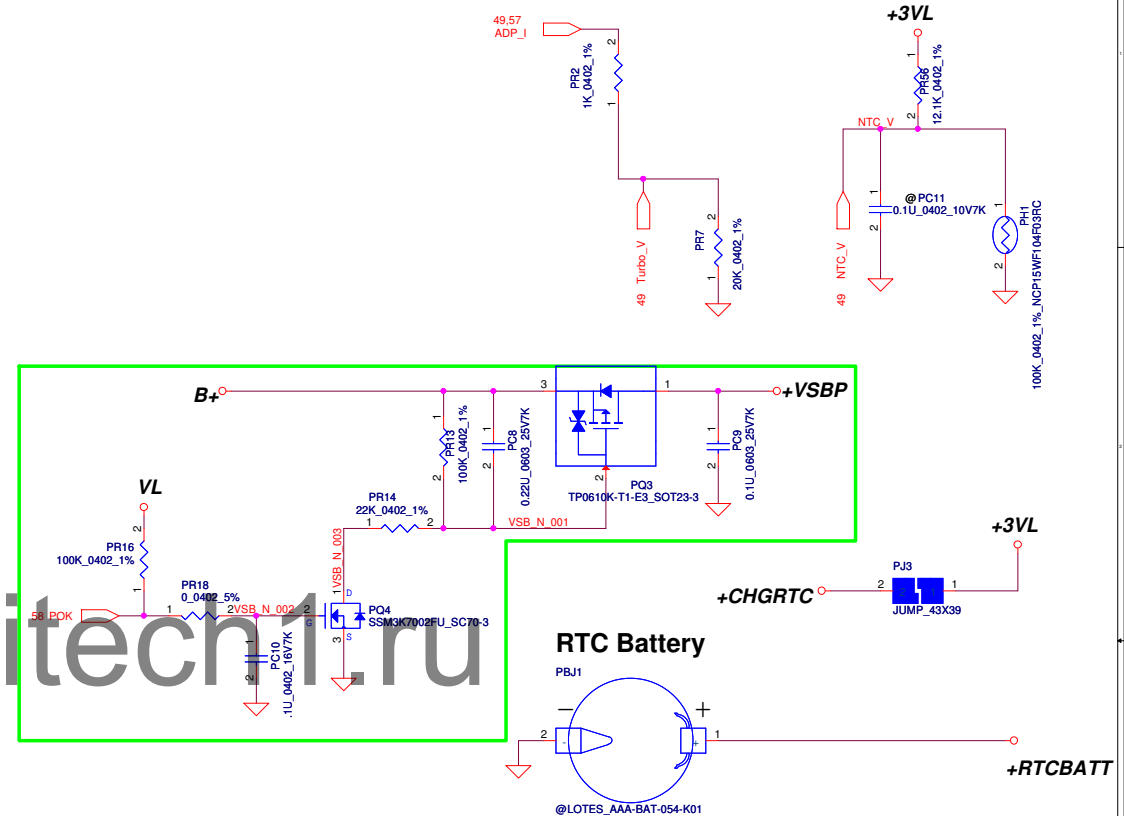


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				Date: Friday, July 13, 2012	Rev 1.0
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DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

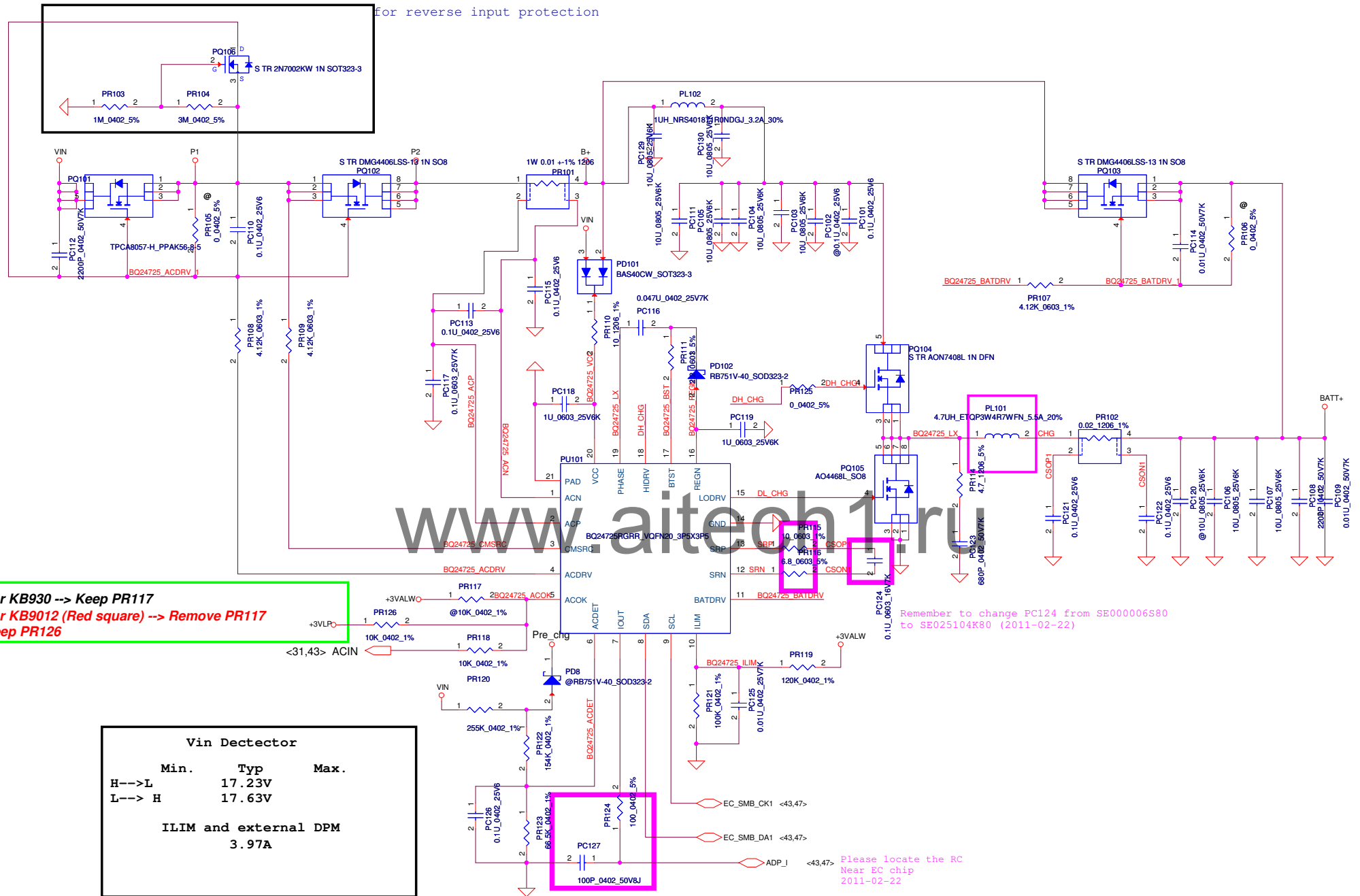


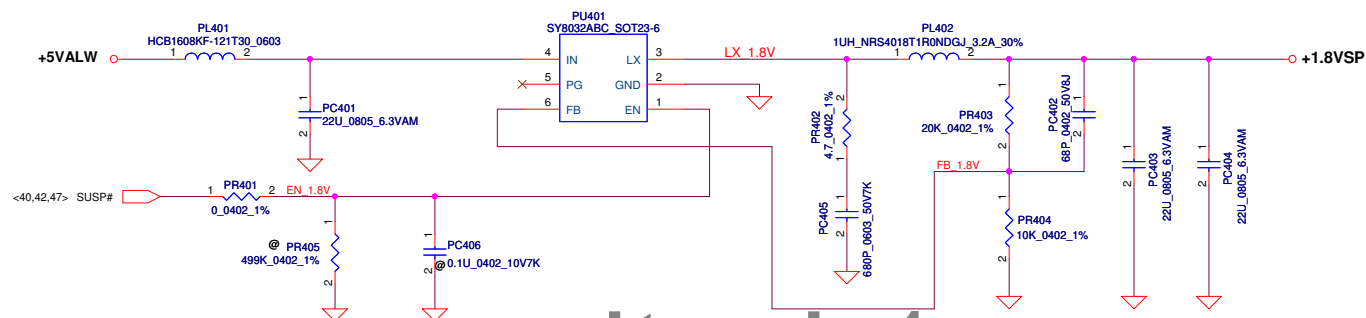
PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



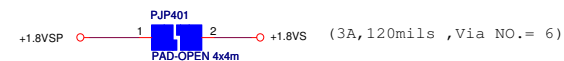
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Size		Document Number	
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For reverse input protection





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				Date:	Friday, July 13, 2012	Sheet 46 of 56

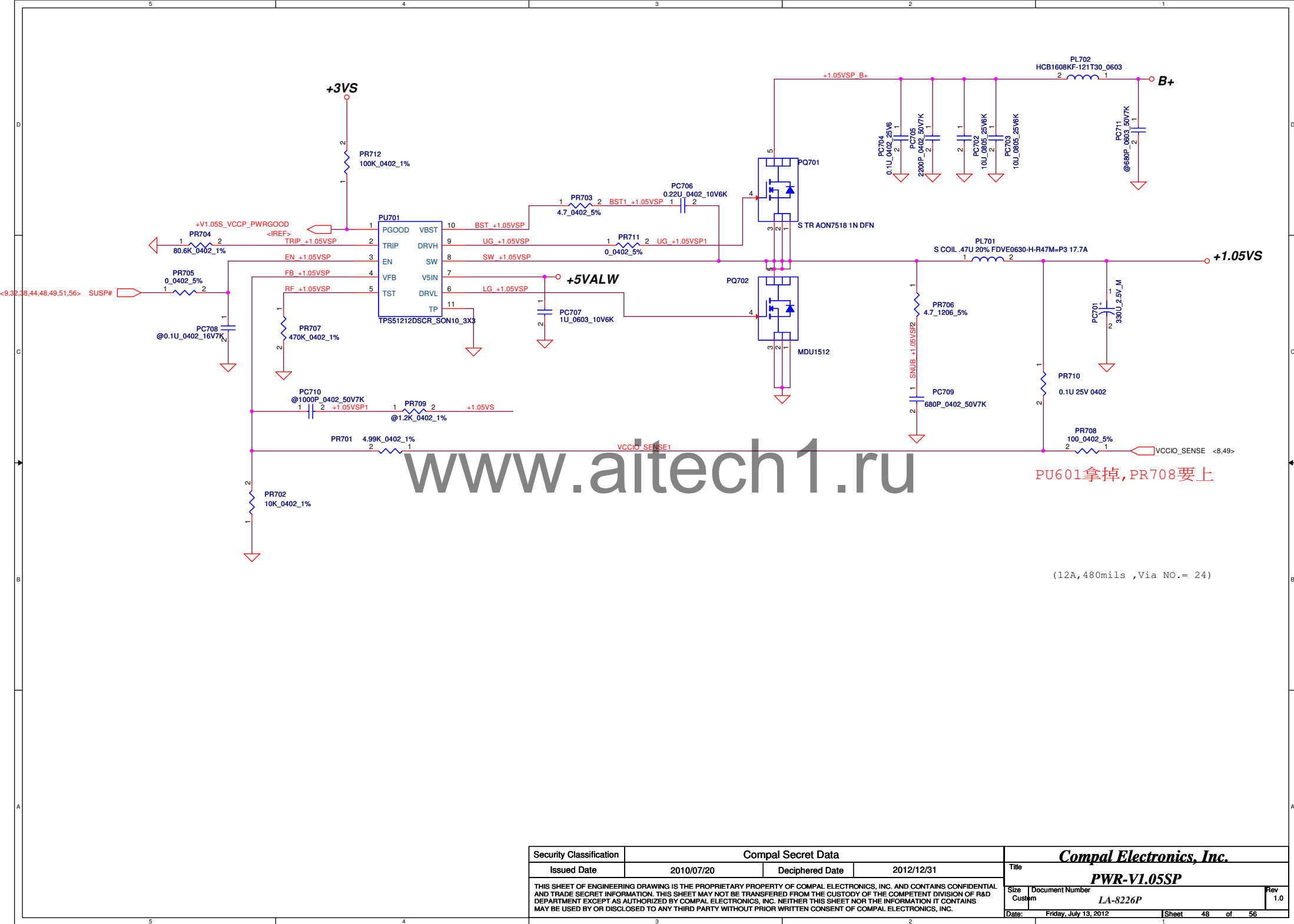


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(8.5A,360mils ,Via NO.= 17)

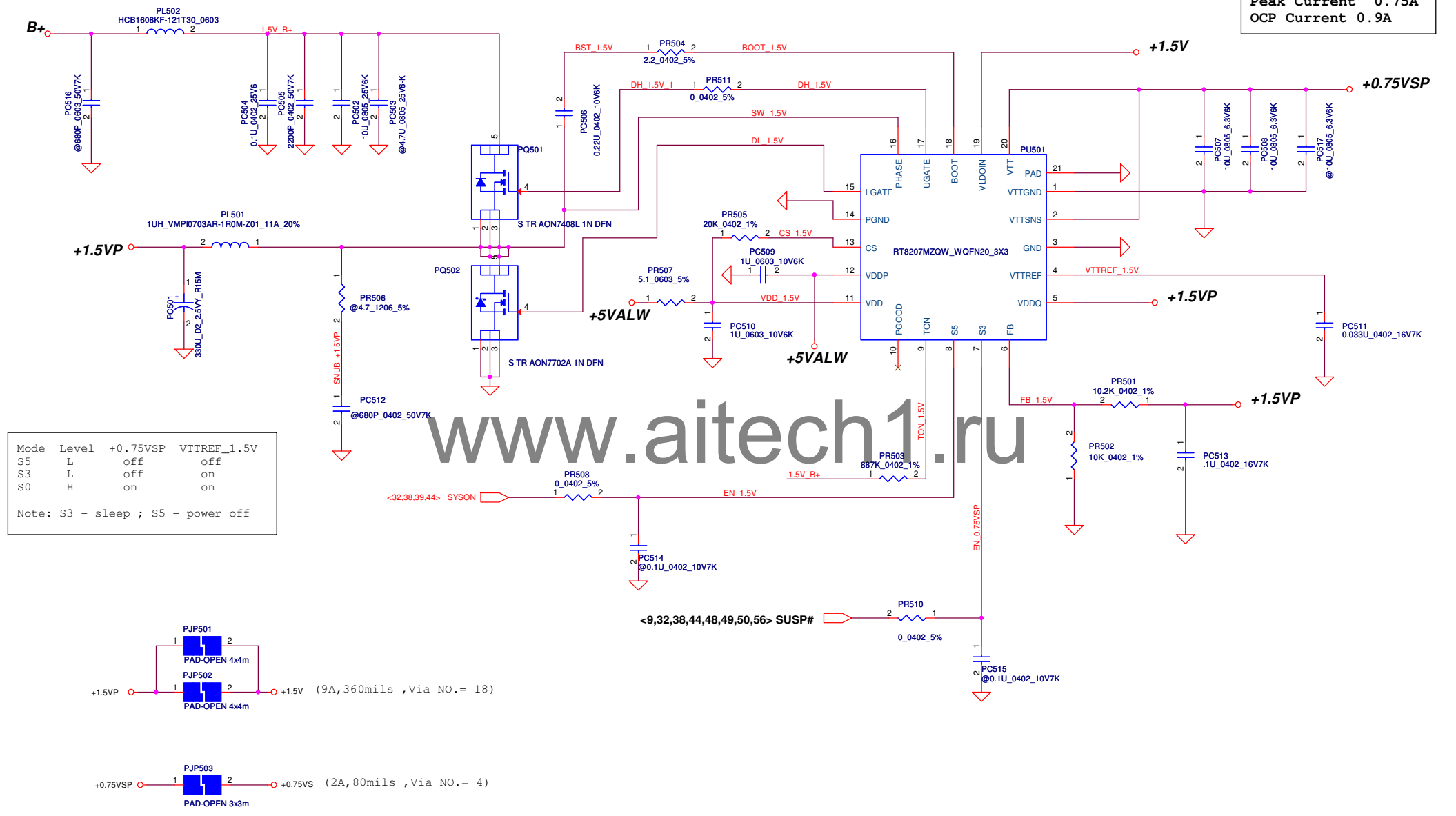
PJP606,PJP607先斷開,確定拿掉PU605再接上

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title PWR-V1.05S VCCP		
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0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

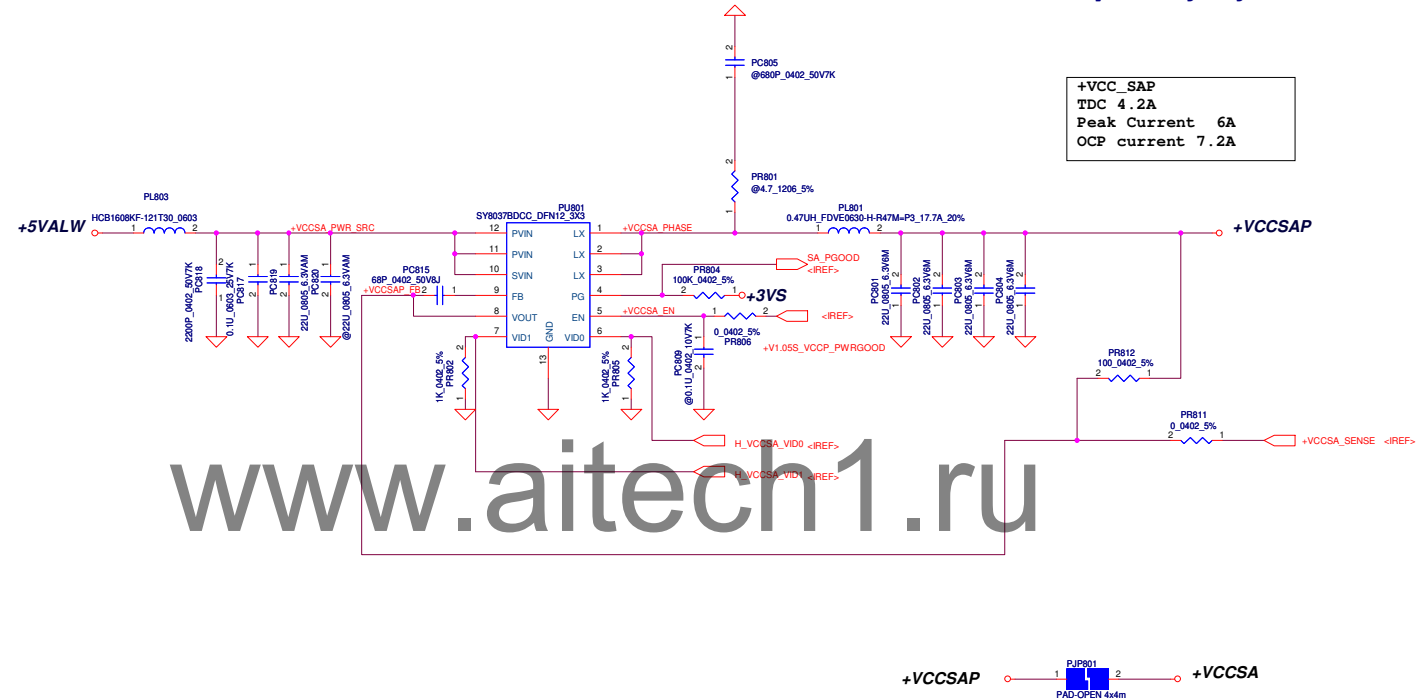


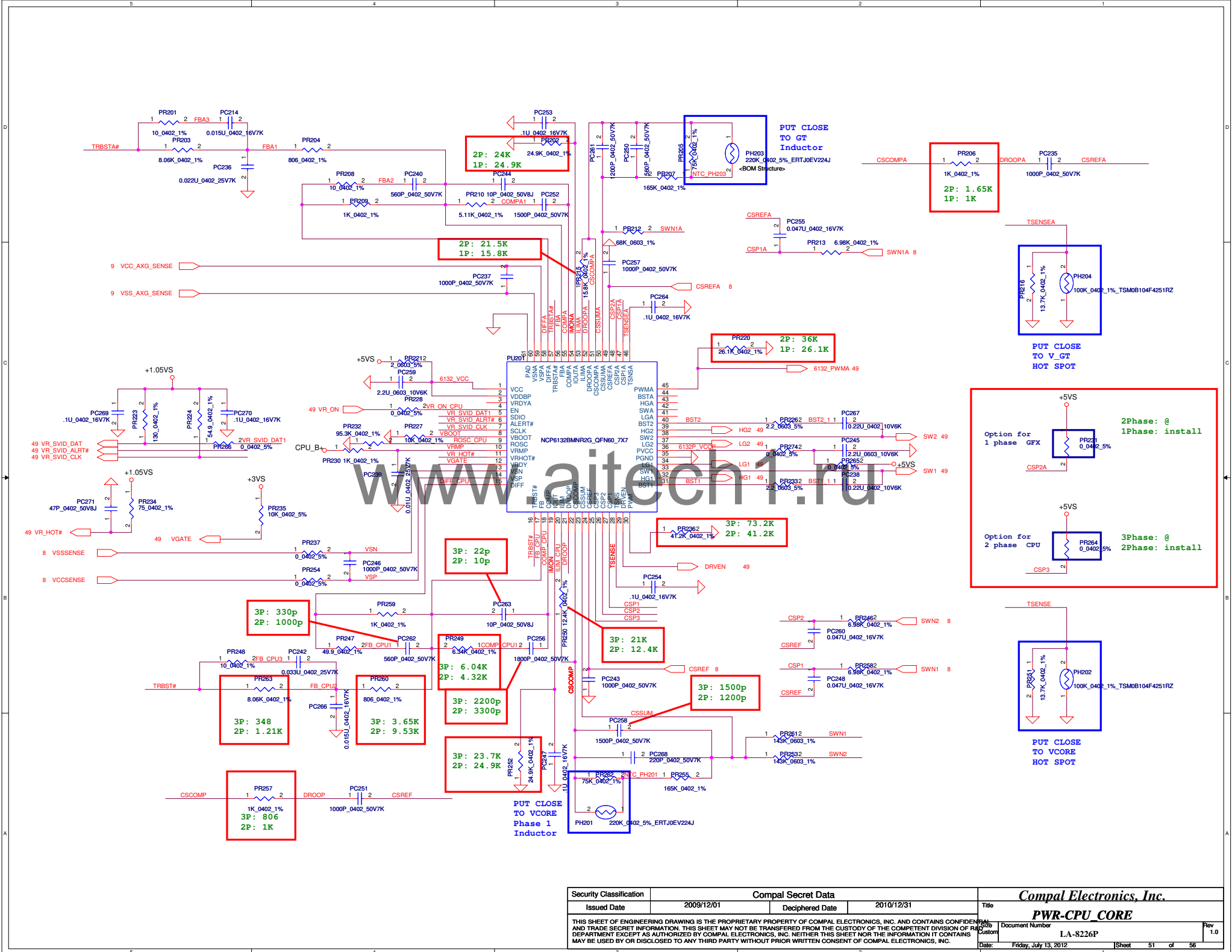
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

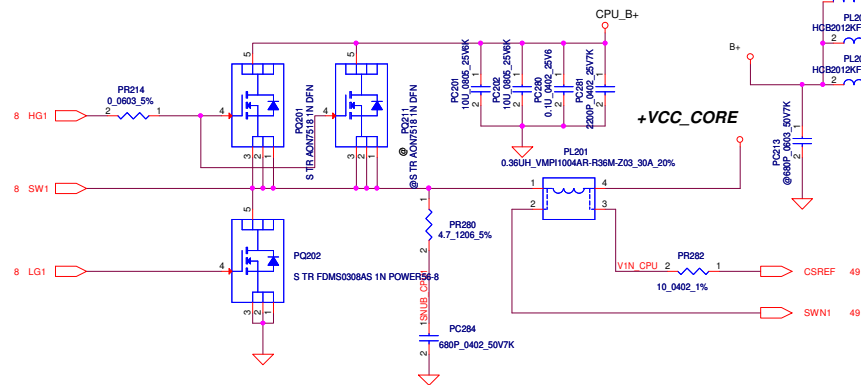
output voltage adjustable network

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```





Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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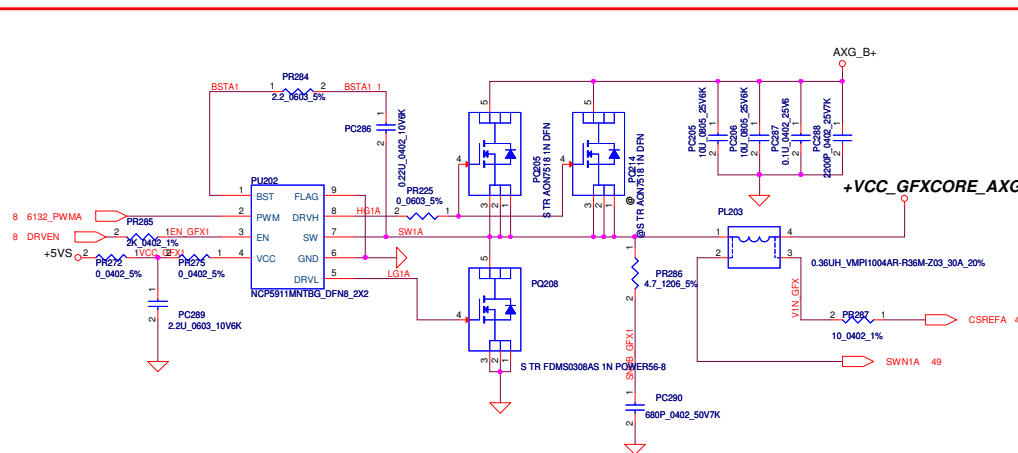
QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=56A
R_LL=1.9m ohm
OCP-110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=33A
R_LL=1.9m ohm
OCP-65A

QC 45W CPU
solution: 3+2
MOS: cpu_core --> 1 (CSD17308) 1 (TPCA8059)
Gfx_core --> 1 (CSD17308) 1 (TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core --> 1 (CSD17308) 1 (TPCA8059)
Gfx_core --> 1 (CSD17308) 1 (TPCA8057)

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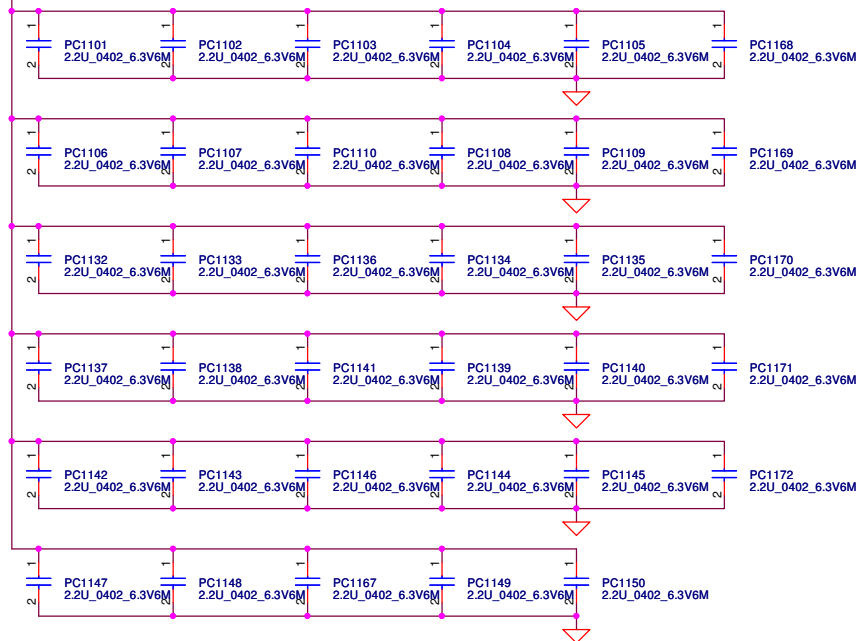


QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

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+VCC_CORE



+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

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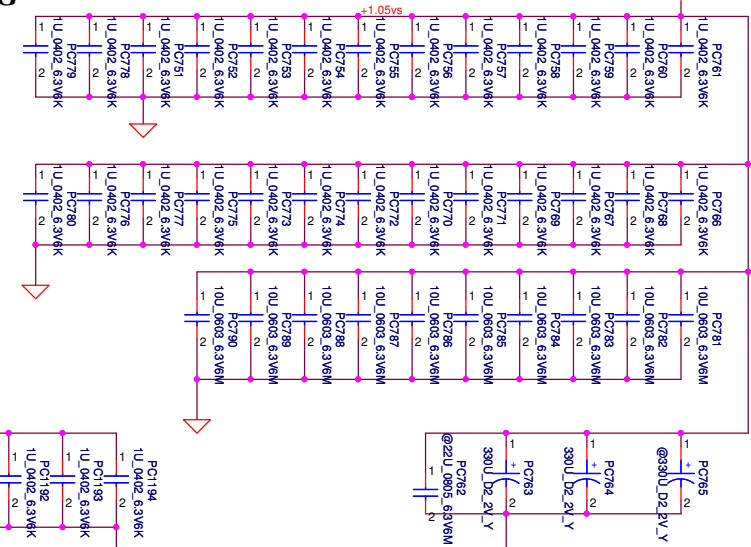
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+VCC_GFXCORE_AXG

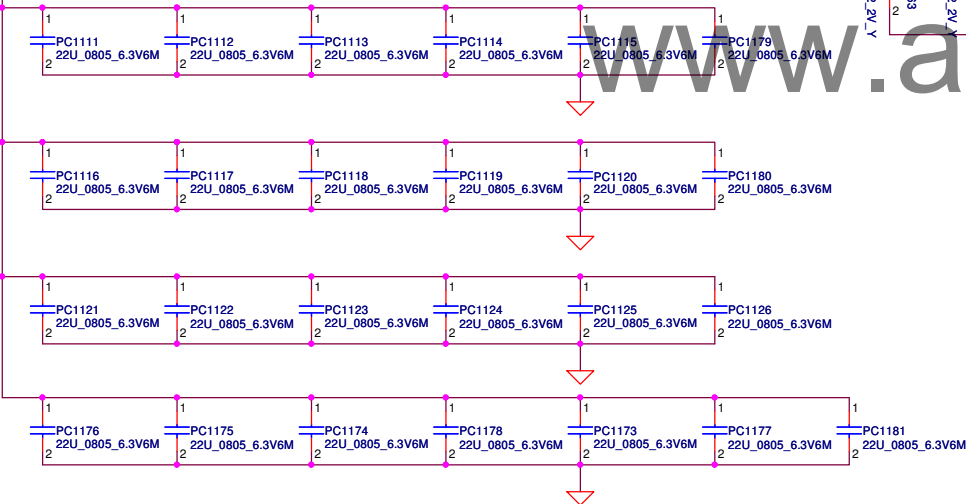
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+VCC_GFXCORE_AXG

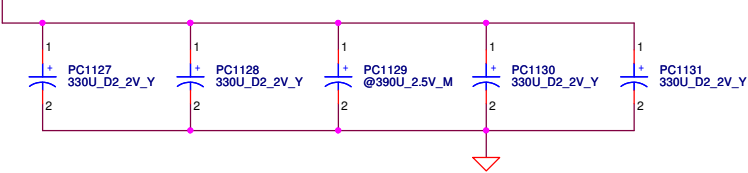
+1.05vs



+VCC_CORE



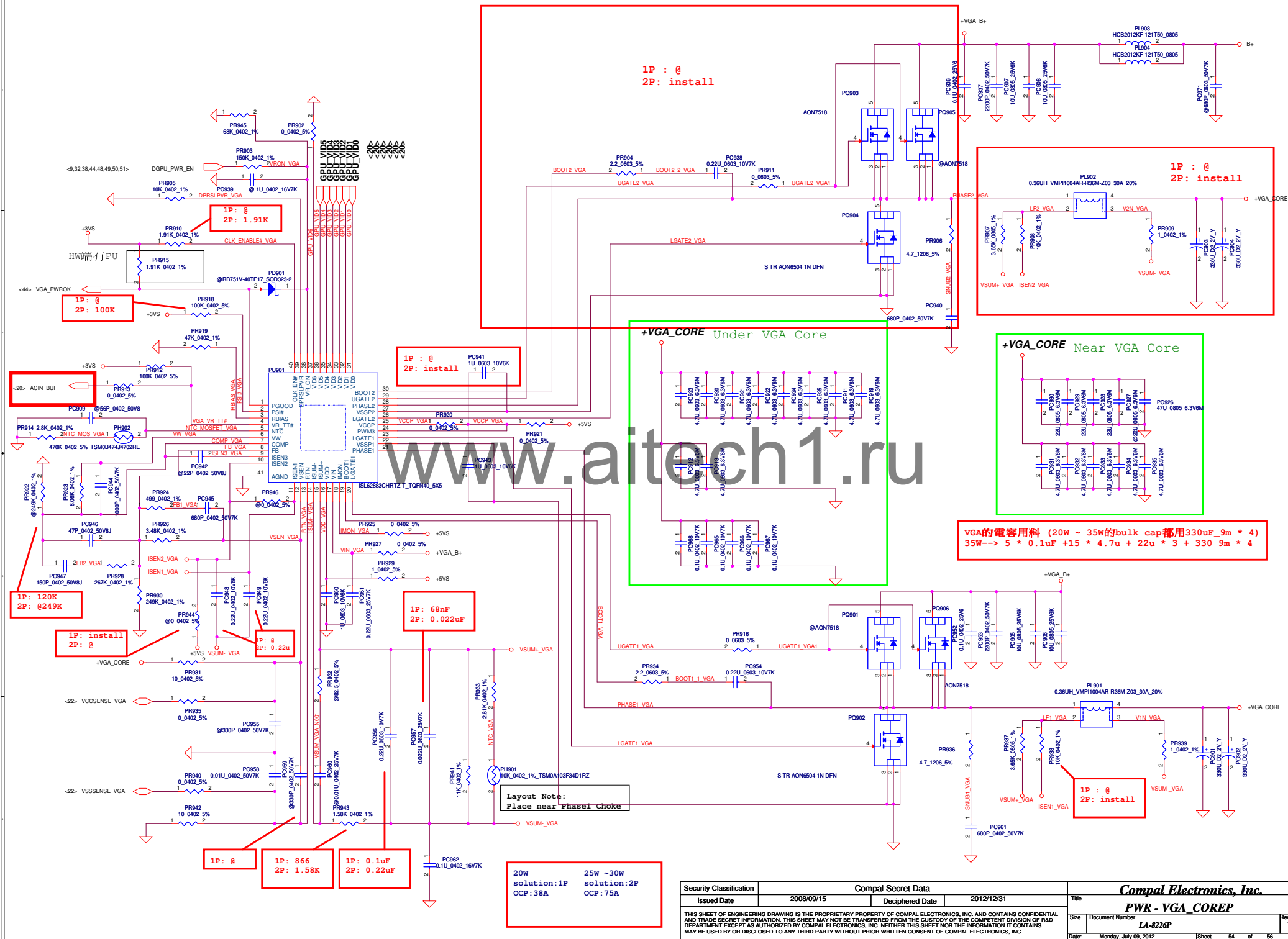
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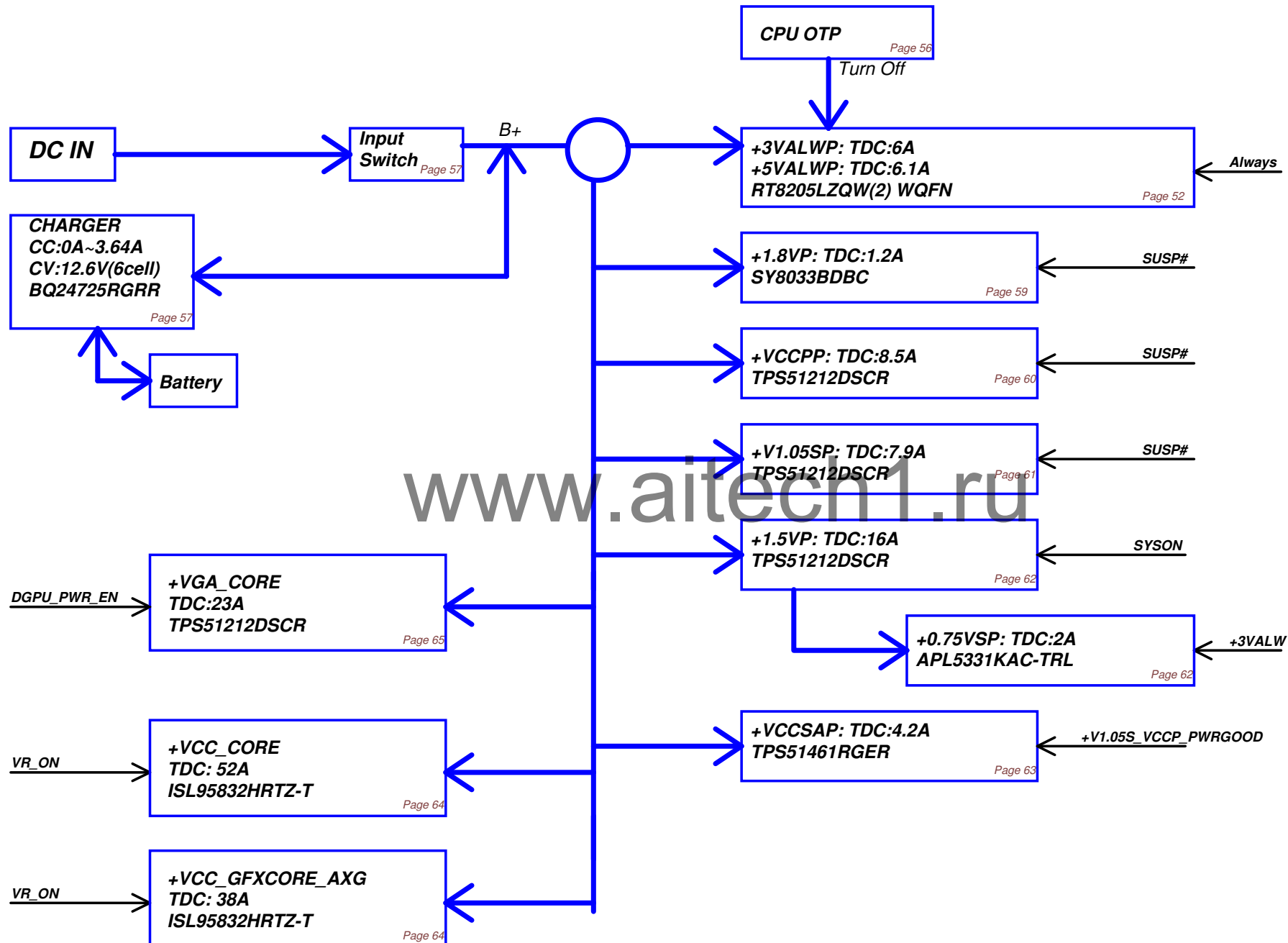
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Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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Power block

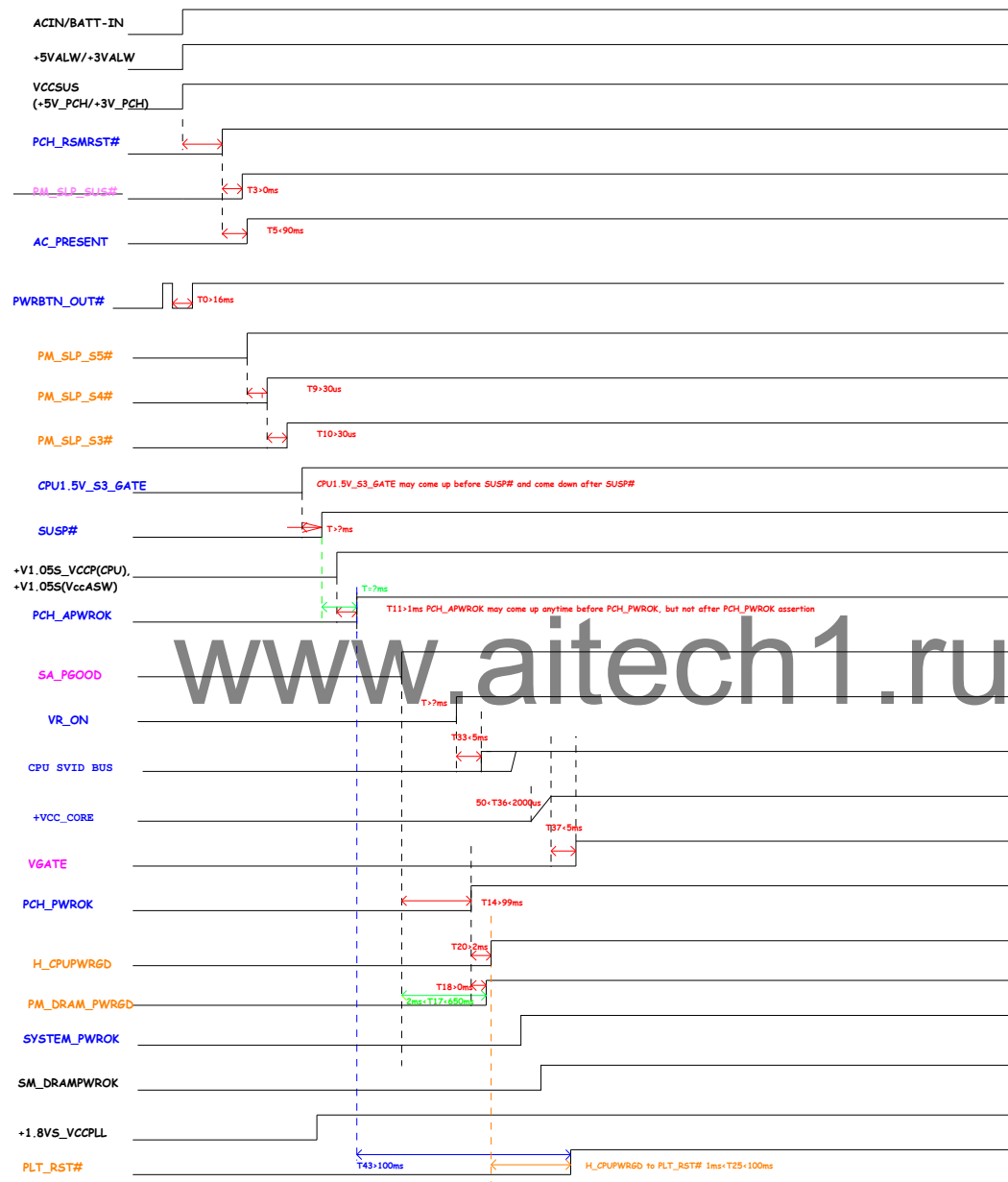


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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		CPU change from socket to BGA 1023	0.1	4~9	CPU change to UCPU1(BGA1023) from JCPU1(socket).	5/28	
		Modify CPU Cap.	0.1	8,9	Change C74,C75 to 1uf/0402 Del C79,C80,C81,C82,C83,C84. Add C243,C239,C151,C177,C219,C157,C181,C237, C153,C192 to 1uF/0402 Add C238,C241,C240,C236,C156,C244,C242,C143 to 10uF/0603 Del C86,C87,C88,C89,C94. Add C245,C246,C254,C248,C249, to 1uF/0402. Add C253,C250,C252,C251,C247 to 10uF/0603.	5/28	
ER02		For Green CLK	0.1	12 13 32 20 43	Add R683 0 ohm. (PCH_32K) Add R637 0 ohm. (PCH_25M) Add R555 0 ohm. (LAN_25M) Add R96 0 ohm. (VGA_27M) Add C89 2.2uF. Add C86,C87 12pF. Add C81 22uF. Add C79,C83,C84,C82,C80 0.1uF. Add Y5 25M. Add U6 SLG3NB300VTR. Add R31 1M. Add R5 22ohm. Add R95,R35 33ohm. Add R30 330ohm. Add R97 0ohm.	5/28	
ER03		Remove reserve components	0.1	33 34 35 38 5,6,13, 17,18	Del C504,C505,C507. Del C655,C656,R681. Del C626,C628,C634,F1,Q53,Q56,R643,R664. Del D30,Q30,R532,R530. Del R267,R43,R750,R278,R290.	5/29	
ER04		Remove ASM1042 (Del page 36) Green CLK VDD change EMI solution	0.1	13,36,37 43 13,32,20	Del ASM1042 . U6 VDD change to +3V_PCH from +LAN_IO. Add R185,R186,R187.(reserve) Add C255,C256,C257.(reserve)	5/30	
ER05		EMI solution	0.1	42	Add C258,C259,C260.(reserve)	5/31	
ER06		BOM modify	0.1	17 15	C180 change to 22uf (SE000000I110). stuff R234 0 ohm	6/4	
ER07		Green CLK modify EMI solution	0.1	42 38	Del R31,R97. Change U6 pin3 voltage to +1.05VS. Add C261.(reserve)	6/4	
ER08		Modify Cap.	0.1	09	Add C262,C263 to 10uf . un-stuff C97,C85,C78 .	6/6	
PR01		Change JDIMM1. footprint	1.0	10	Change JDIMM1 footprint.(TYCO_2-2013298-1_204P)	7/4	
PR02		Swap Resistor	1.0	07	Swap R48 & R46.	7/5	
PR03		EMI solution / GCLK	1.0	35,42	Add C655,C656,C674 to 2.2pf . C87 change to 15pf. R95 change to 0 ohm.		

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